FIG. 1

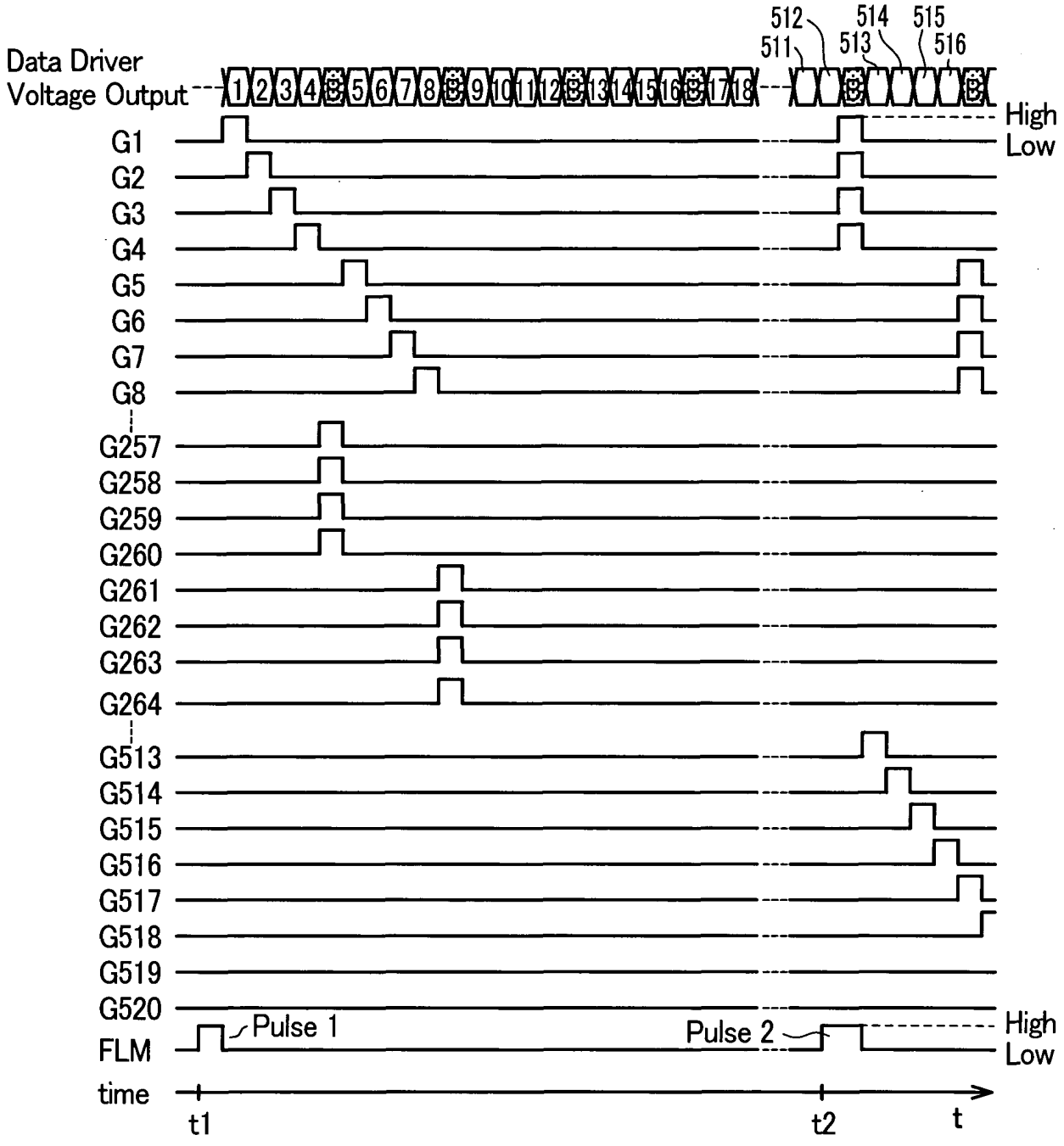

Data Driver
Voltage Output
512
514
515
511
513
516
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
High
Low
G1
G2
G3
G4
G5
G6
G7
G8
G257
G258
G259
G260
G261
G262
G263
G264
G513
G514
G515
G516
G517
G518
G519
G520
FLM
Pulse 1
Pulse 2
High
Low
time
t1
t2
t

FIG. 2

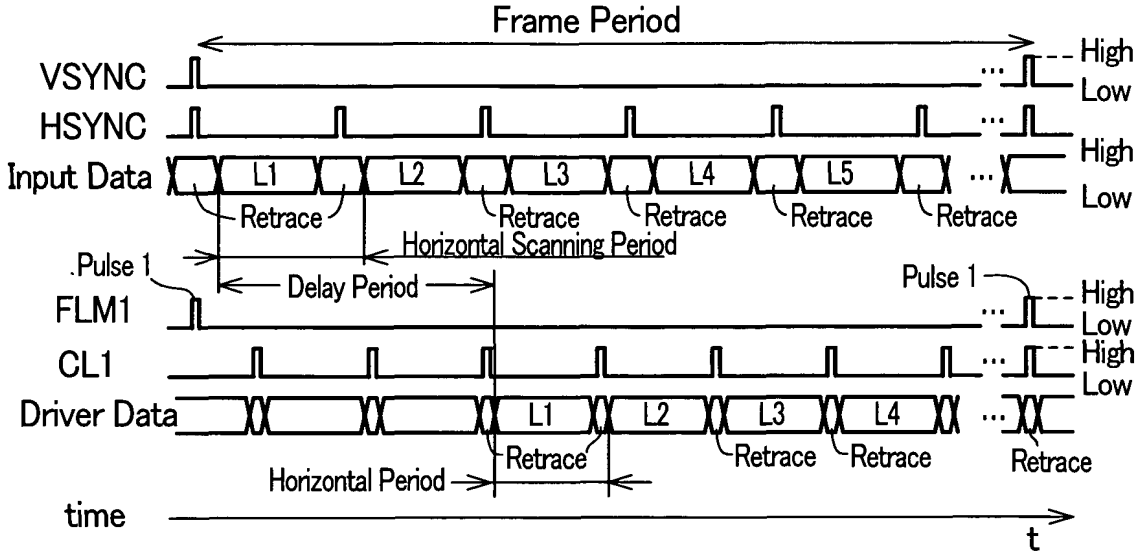

Frame Period
VSYNC
HSYNC
Input Data
L1
L2
L3
L4
L5
Retrace
Horizontal Scanning Period
Pulse 1
Delay Period
FLM1
CL1
Driver Data
Horizontal Period
time
t
High
Low

FIG. 3

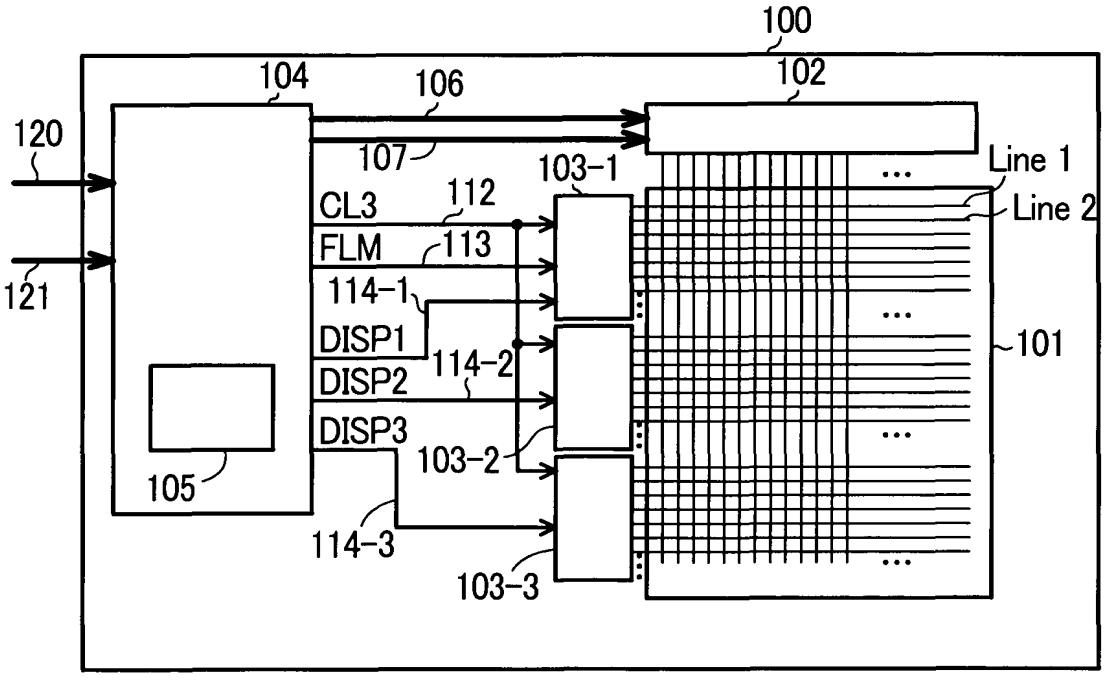

100
102
104
106
107
120
121
103-1
112
CL3
FLM
113
114-1
DISP1
114-2
DISP2
DISP3
103-2
114-3
103-3
105
Line 1
Line 2
101

FIG. 4

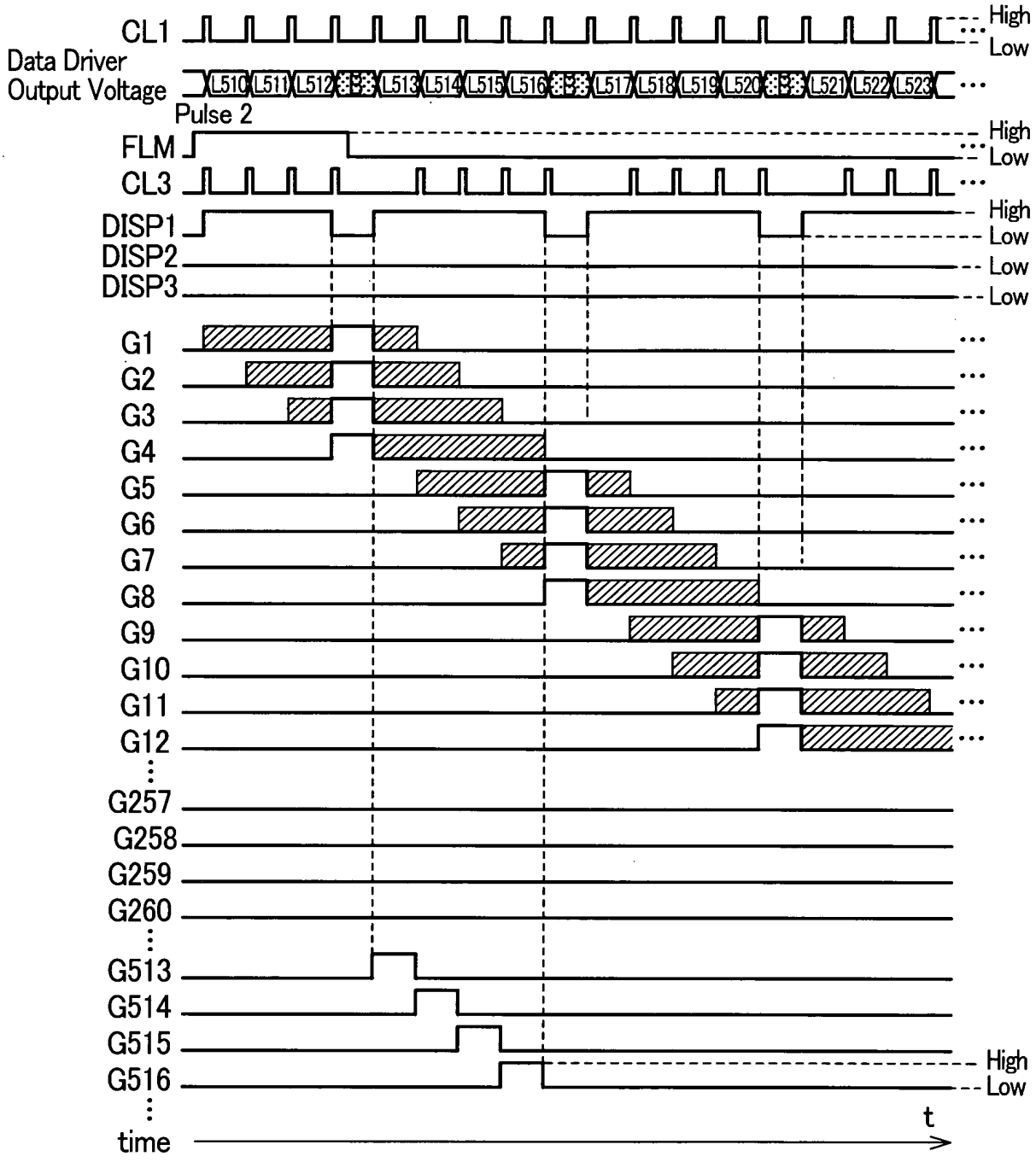

CL1
High
Low
Data Driver
Output Voltage
L510
L511
L512
L513
L514
L515
L516
L517
L518
L519
L520
L521
L522
L523
Pulse 2
FLM
High
Low
CL3
DISP1
High
Low
DISP2
Low
DISP3
Low
G1
G2
G3
G4
G5
G6
G7
G8
G9
G10
G11
G12
G257
G258
G259
G260
G513
G514
G515
G516
High
Low
t
time

FIG. 5

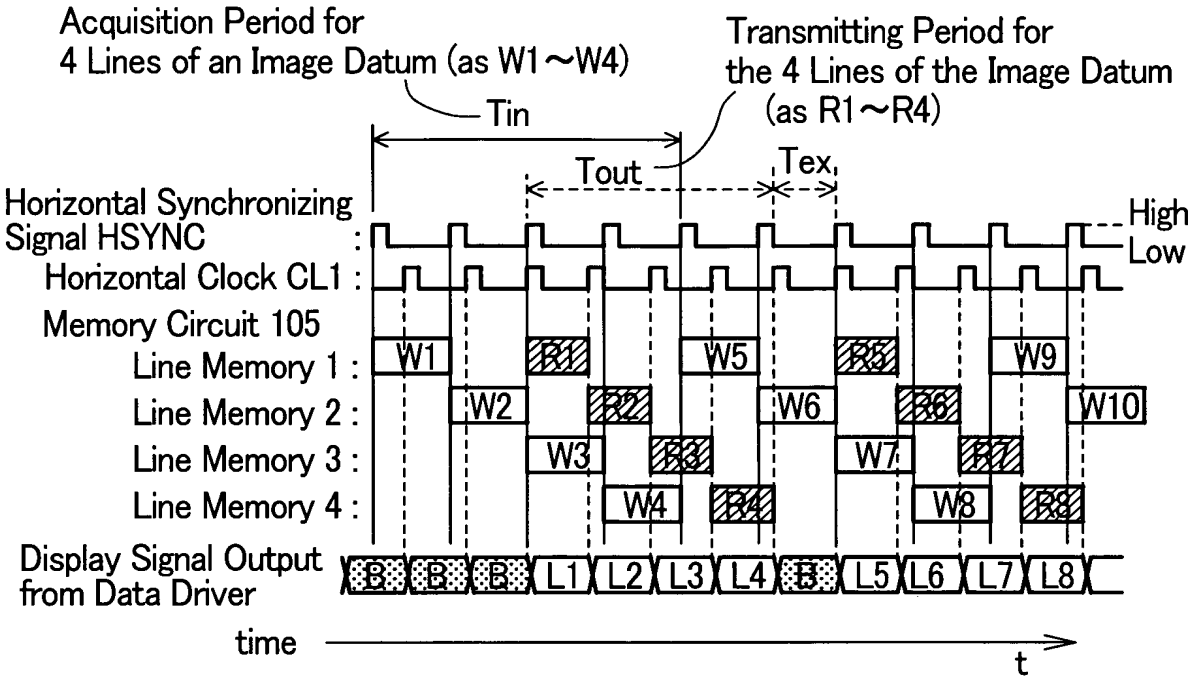

Acquisition Period for
4 Lines of an Image Datum (as W1～W4)
Transmitting Period for
the 4 Lines of the Image Datum
(as R1～R4)
Tin
Tout
Tex
Horizontal Synchronizing
Signal HSYNC :
Horizontal Clock CL1 :
Memory Circuit 105
Line Memory 1 :
Line Memory 2 :
Line Memory 3 :
Line Memory 4 :
High
Low
W1
W2
W3
W4
W5
W6
W7
W8
W9
W10
Display Signal Output
from Data Driver
B
L1
L2
L3
L4
L5
L6
L7
L8
time
t

FIG. 6

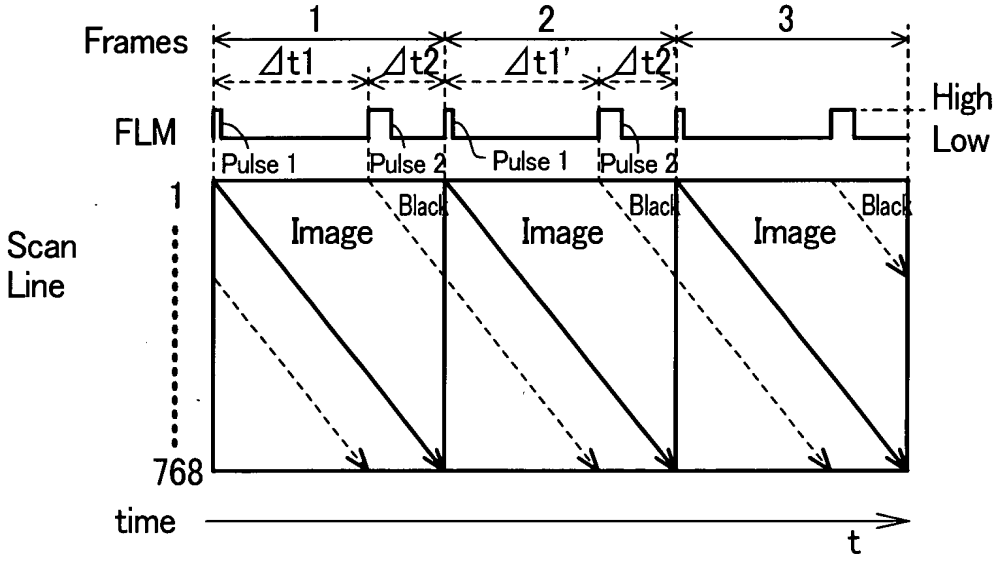

Frames
1
2
3
Δt1
Δt2
Δt1'
Δt2'
FLM
High
Low
Pulse 1
Pulse 2
Pulse 1
Pulse 2
Scan
Line
1
768
Image
Black
Image
Black
Image
Black
time
t

FIG. 7

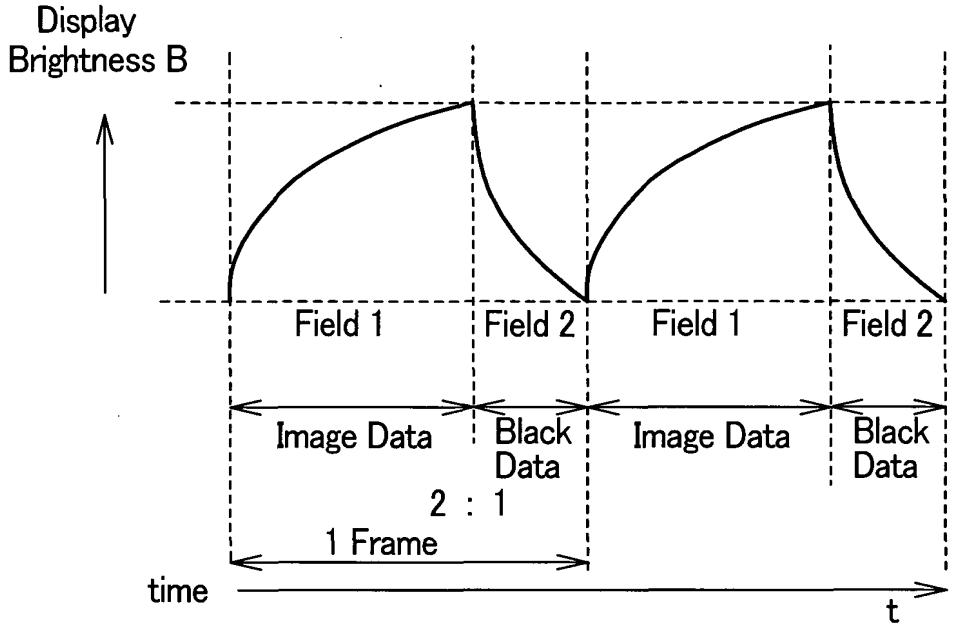

Display
Brightness B
Field 1
Field 2
Field 1
Field 2
Image Data
Black
Data
Image Data
Black
Data
2 : 1
1 Frame
time
t

FIG. 8

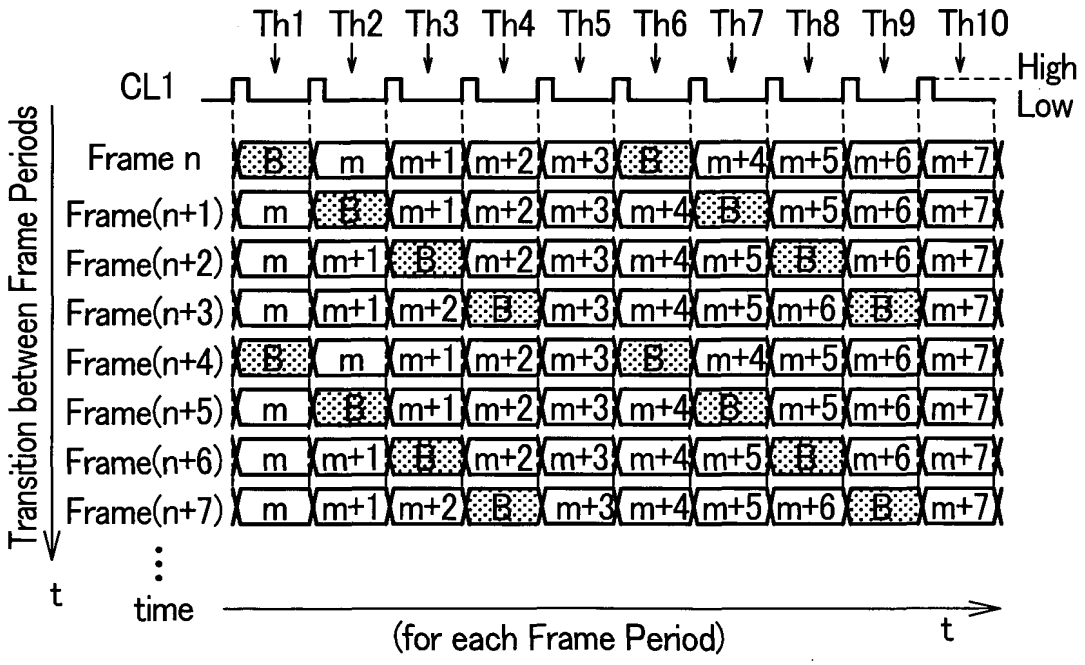

Th1
Th2
Th3
Th4
Th5
Th6
Th7
Th8
Th9
Th10
CL1
High
Low
Transition between Frame Periods
Frame n
Frame(n+1)
Frame(n+2)
Frame(n+3)
Frame(n+4)
Frame(n+5)
Frame(n+6)
Frame(n+7)
B
m
m+1
m+2
m+3
m+4
m+5
m+6
m+7
t
time
(for each Frame Period)
t

FIG. 9

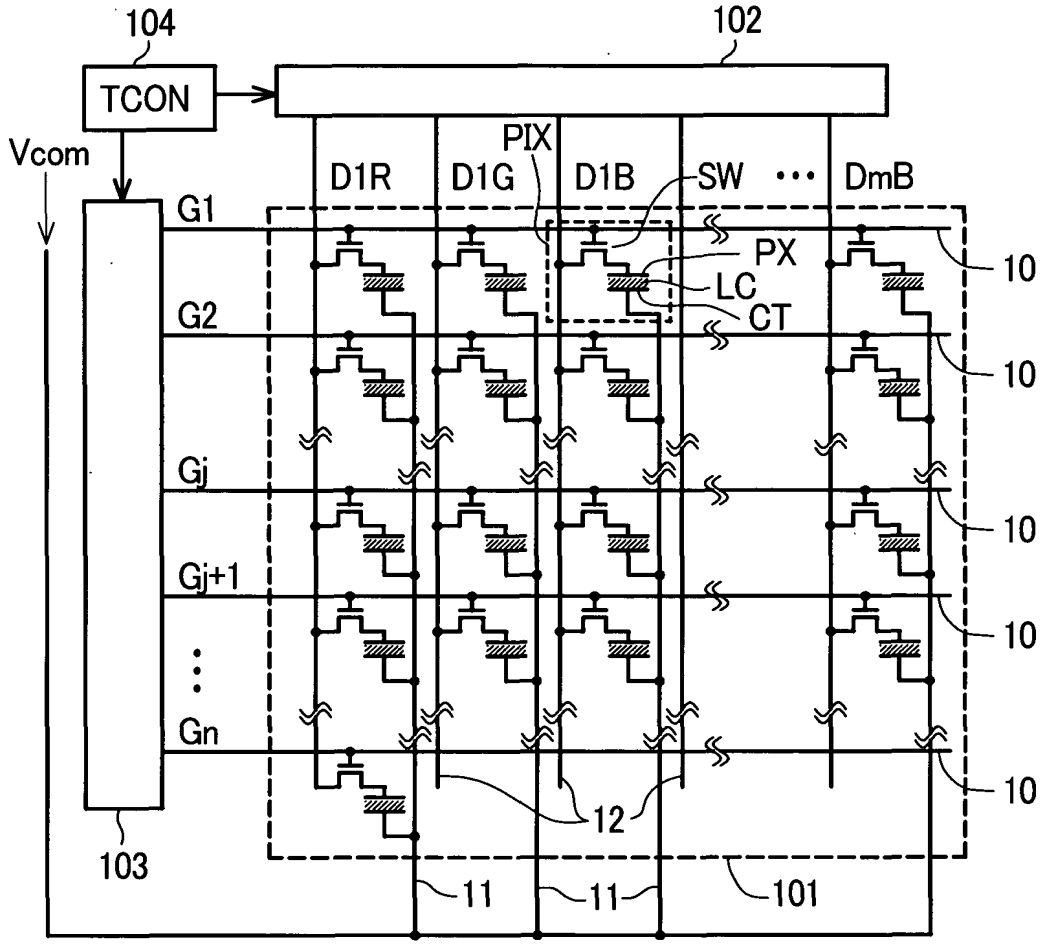

104
102
TCON
Vcom
PIX
D1R
D1G
D1B
SW
DmB
G1
G2
Gj
Gj+1
Gn
PX
LC
CT
10
12
11
101
103

FIG. 10

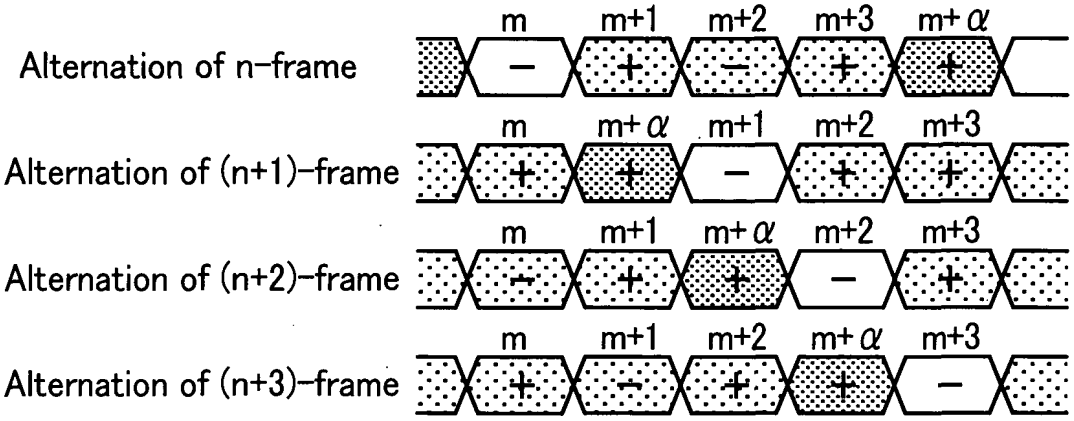

Alternation of n-frame
Alternation of (n+1)-frame
Alternation of (n+2)-frame
Alternation of (n+3)-frame
m
m+1
m+2
m+3
m+α

FIG. 11

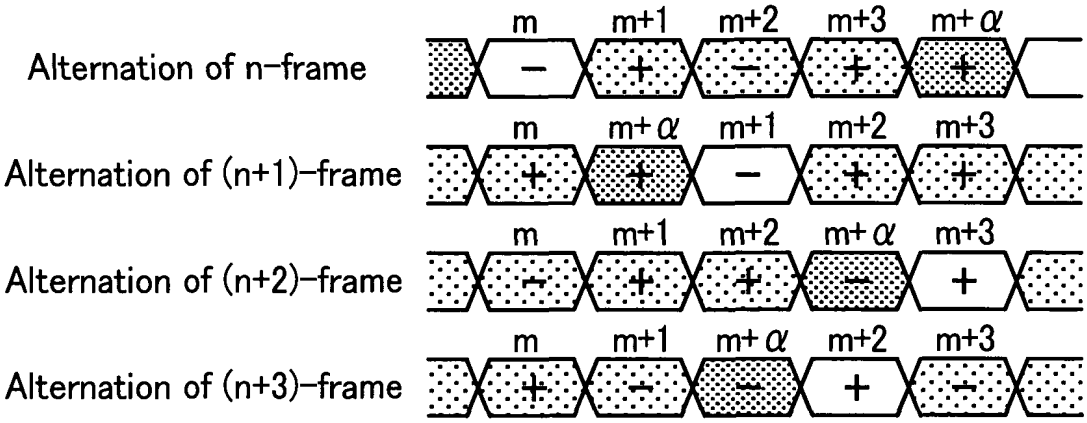


FIG. 12

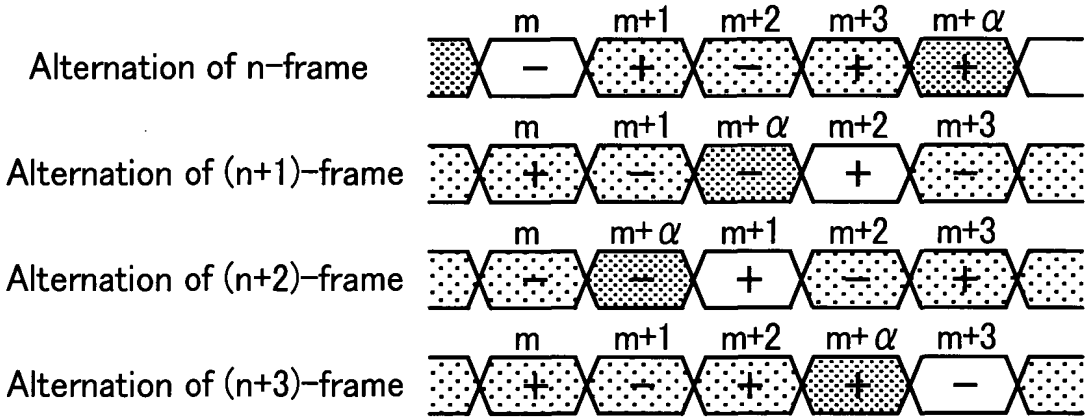


FIG. 13

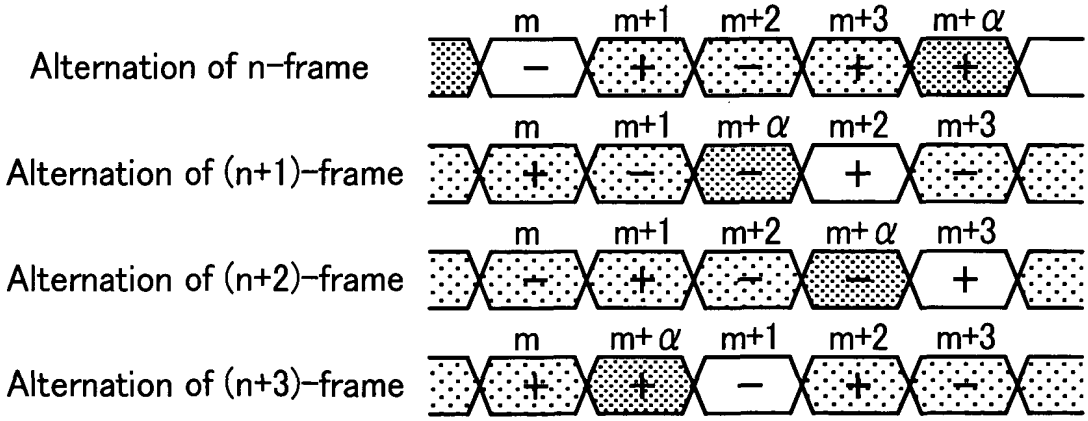


FIG. 14

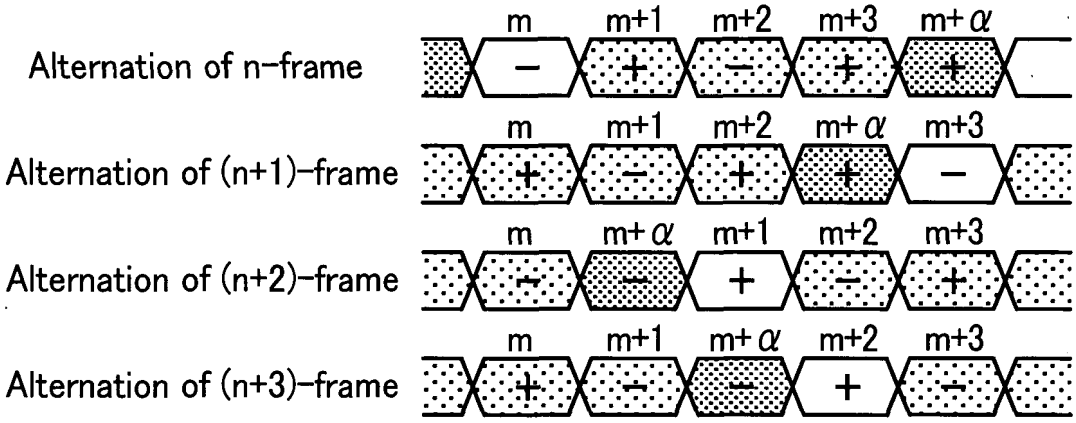


FIG. 15

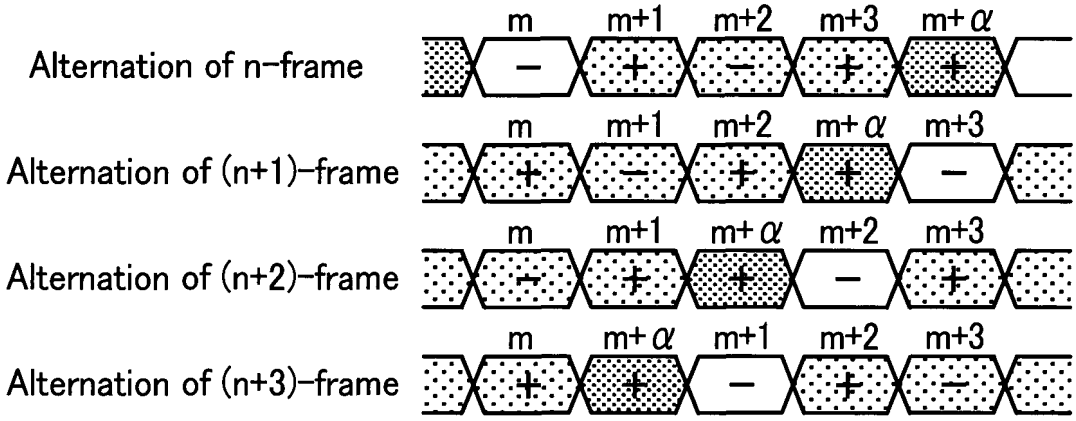


FIG. 16

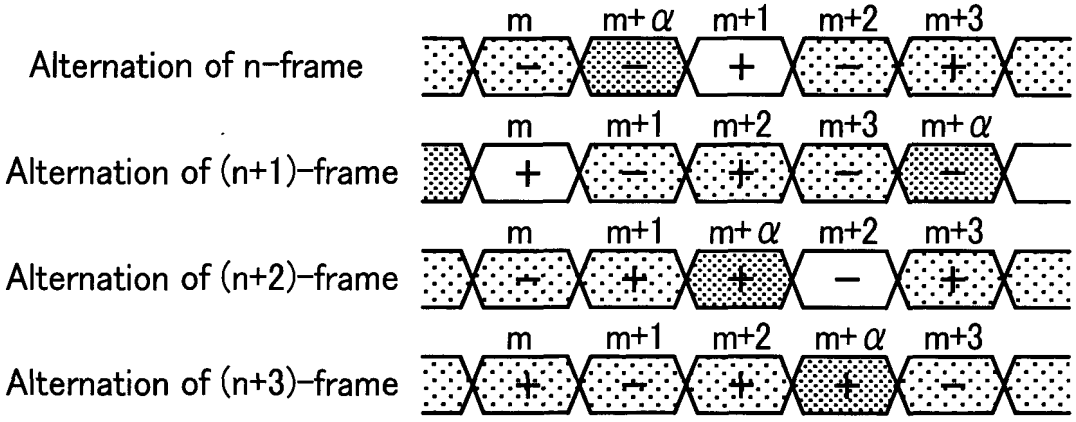


FIG. 17

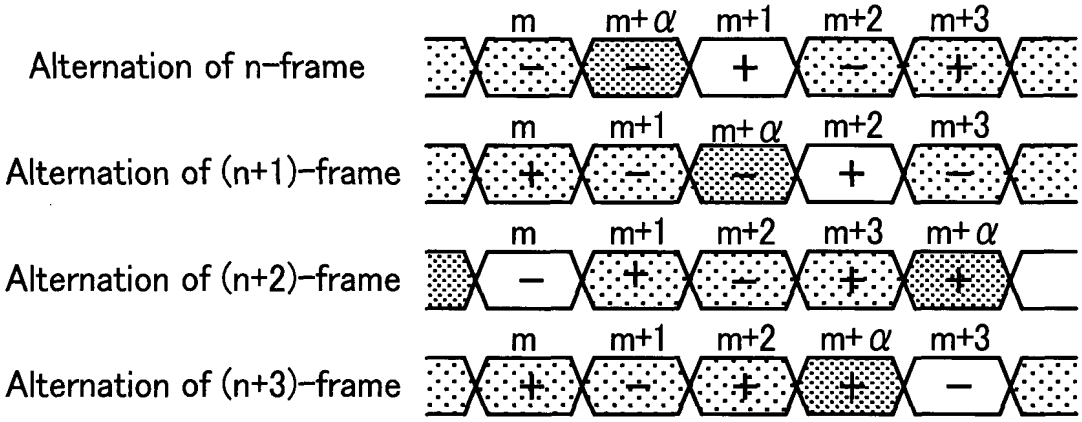


FIG. 18

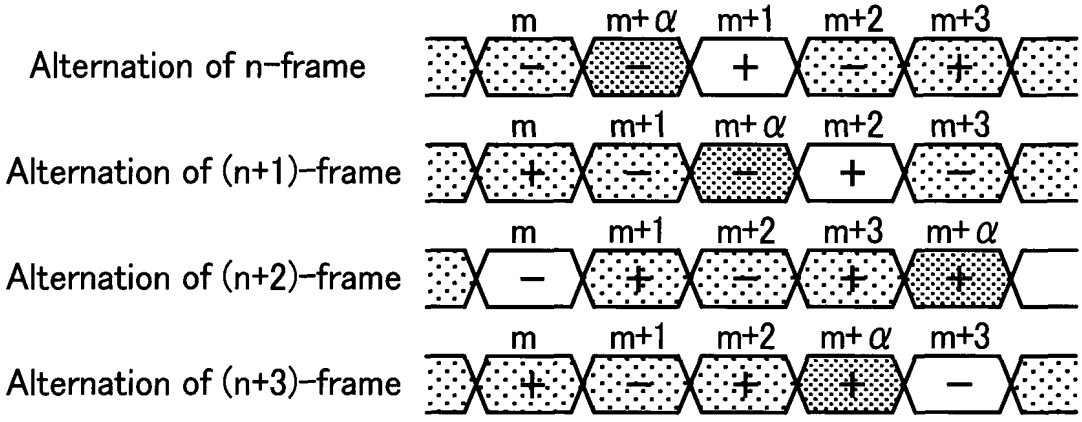


FIG. 19

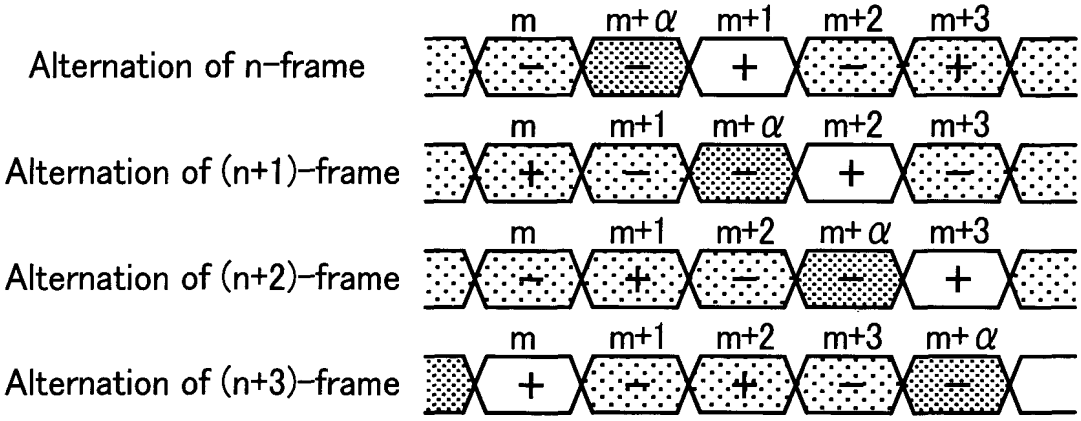


FIG. 20

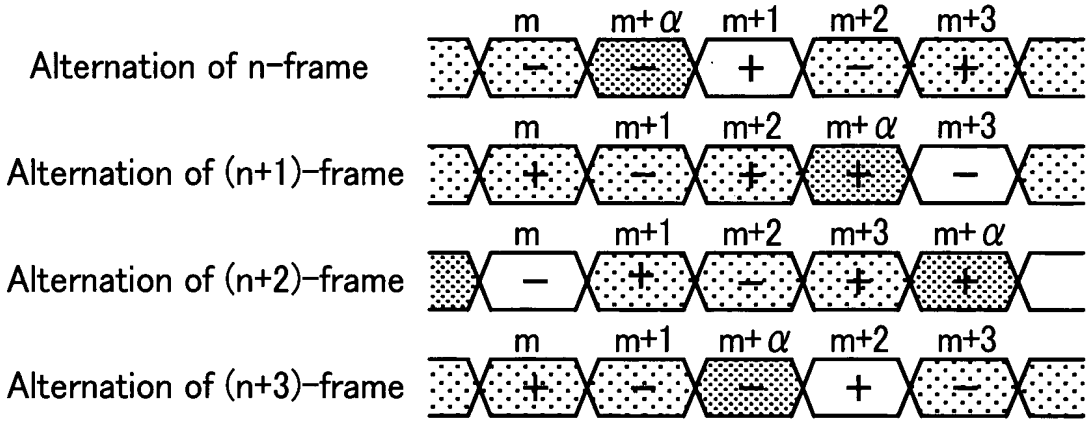


FIG. 21

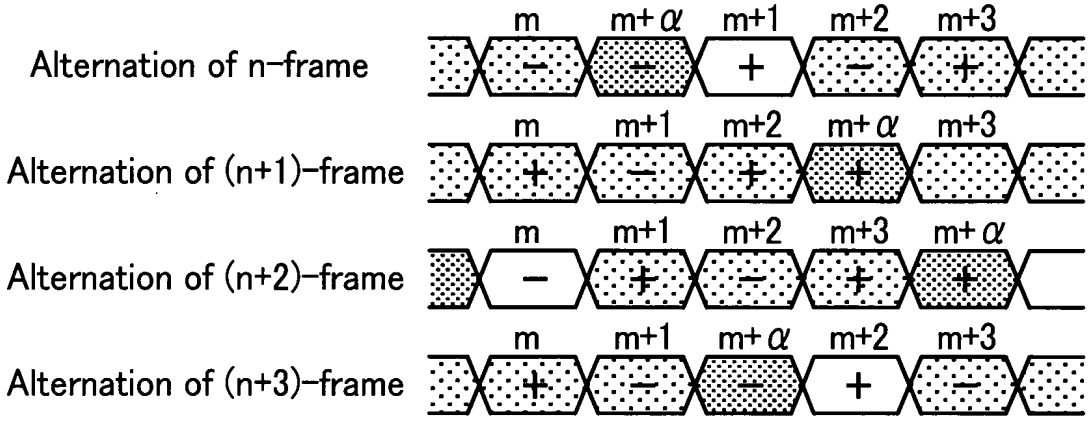


FIG. 22

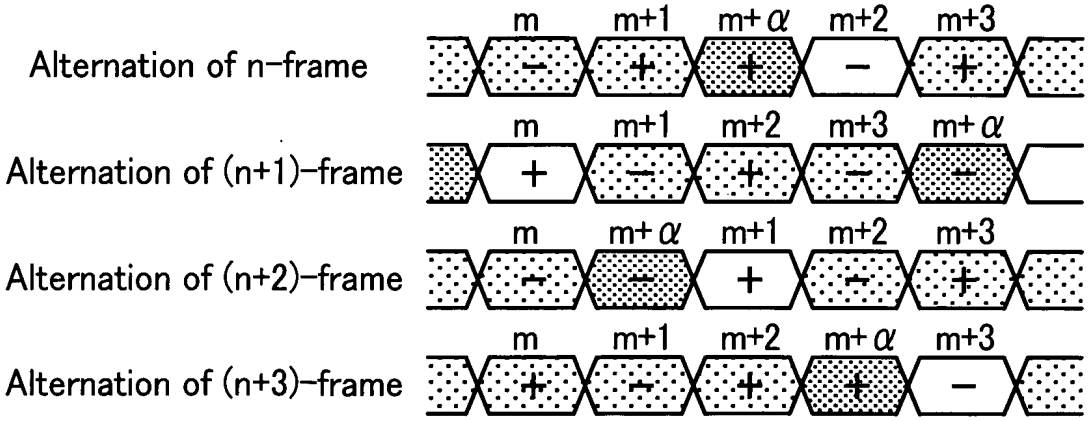


FIG. 23

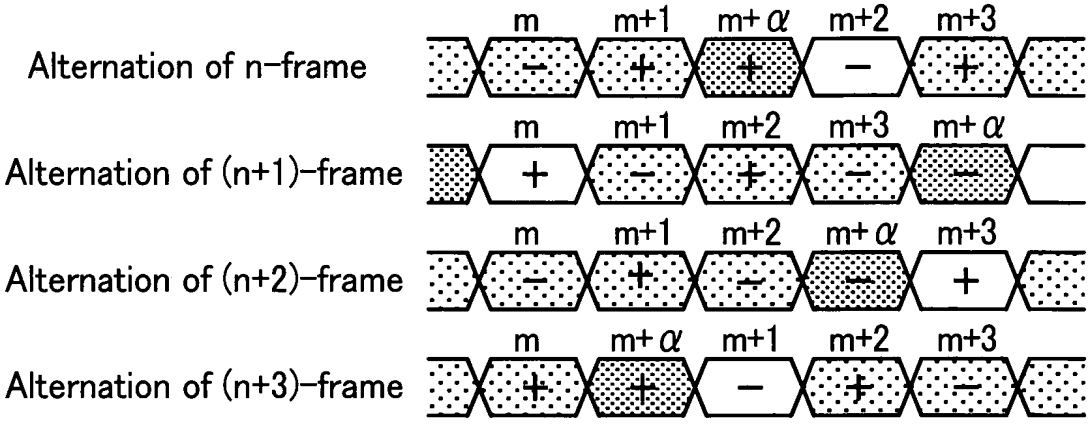


FIG. 24

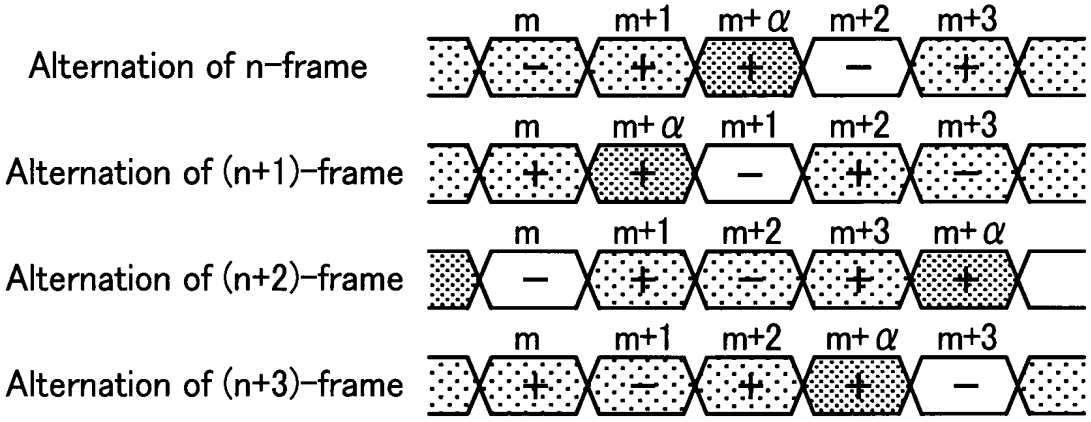


FIG. 25

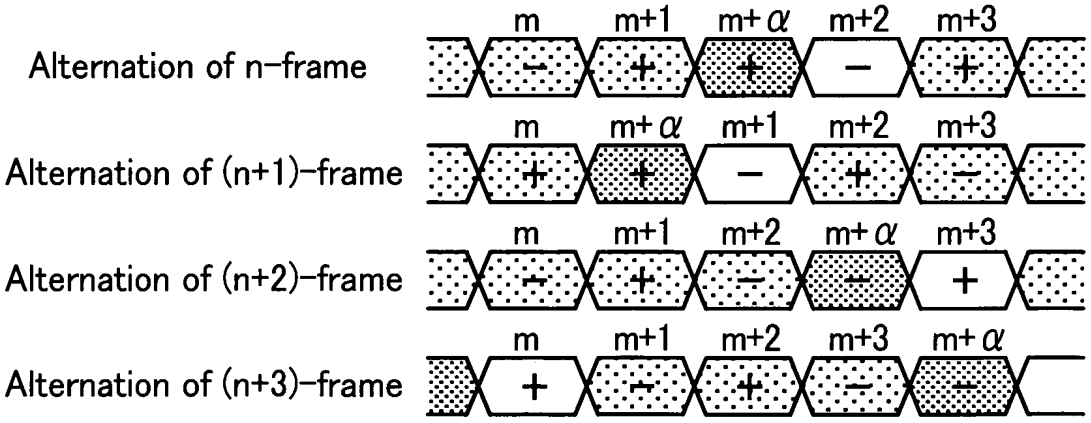


FIG. 26

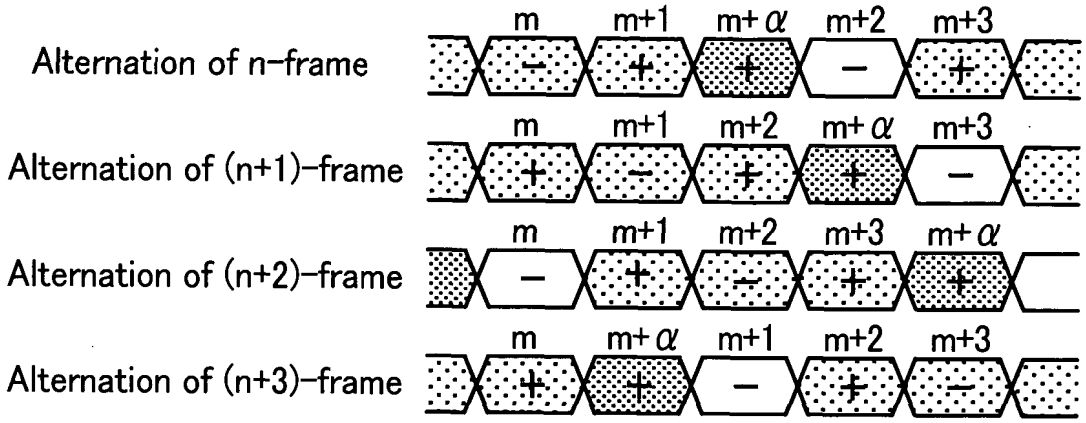


FIG. 27

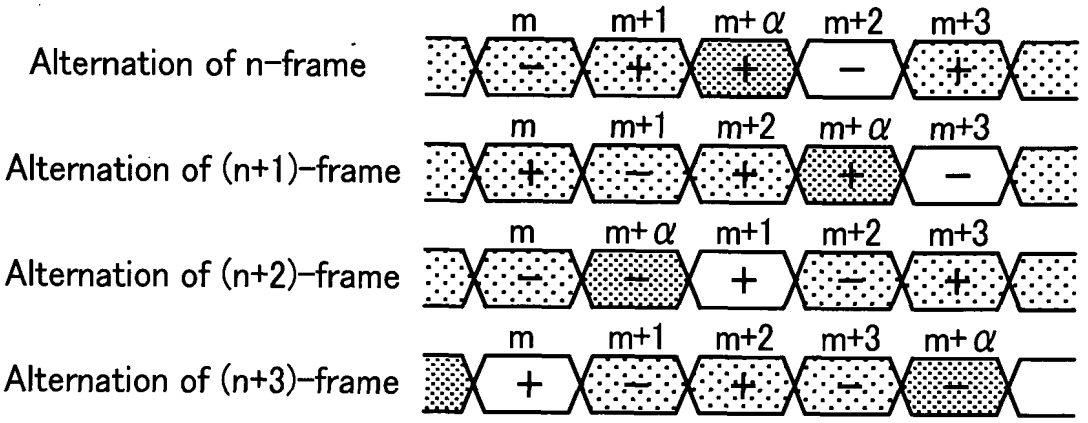


FIG. 28

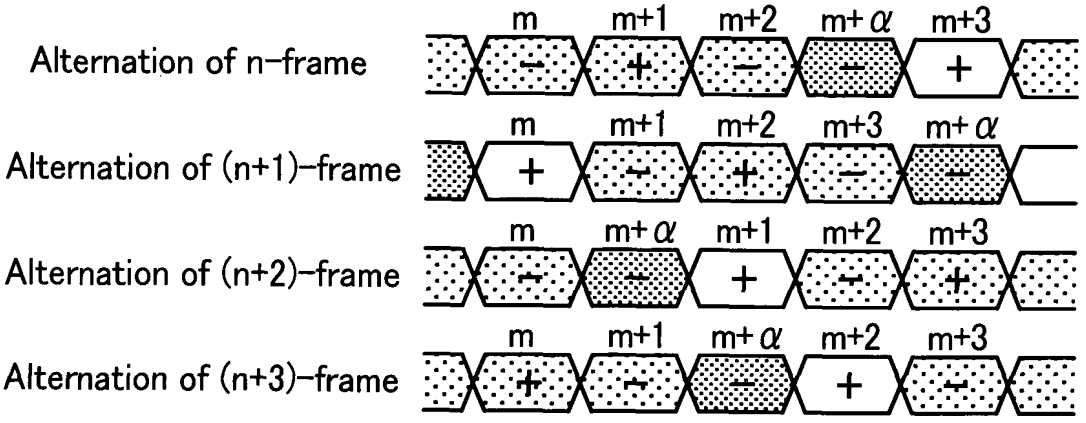


FIG. 29

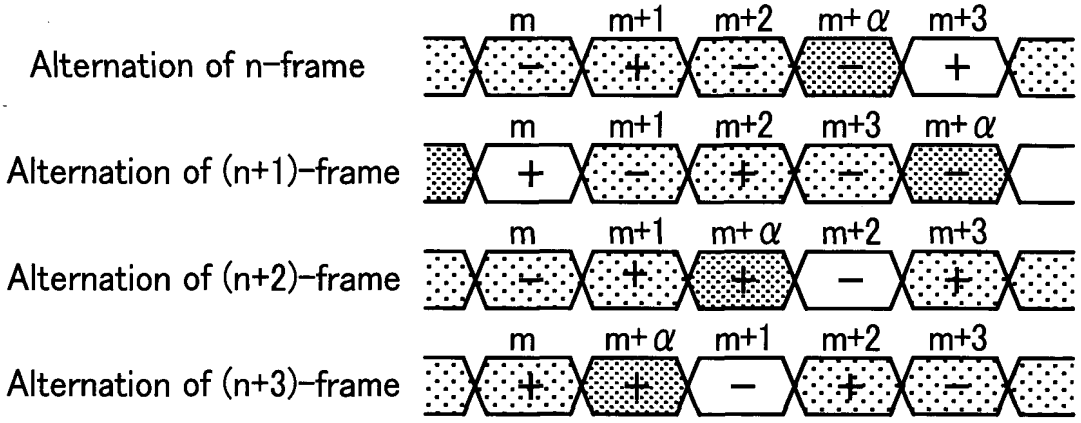


FIG. 30

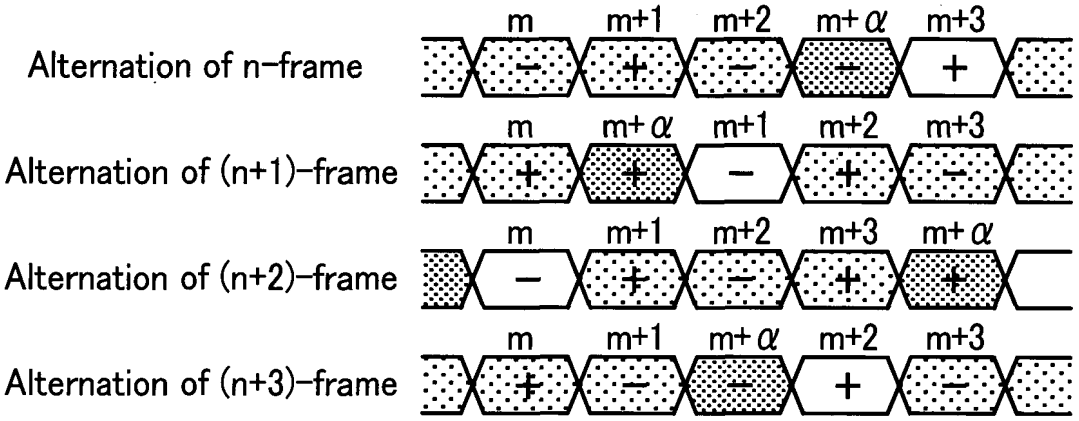


FIG. 31

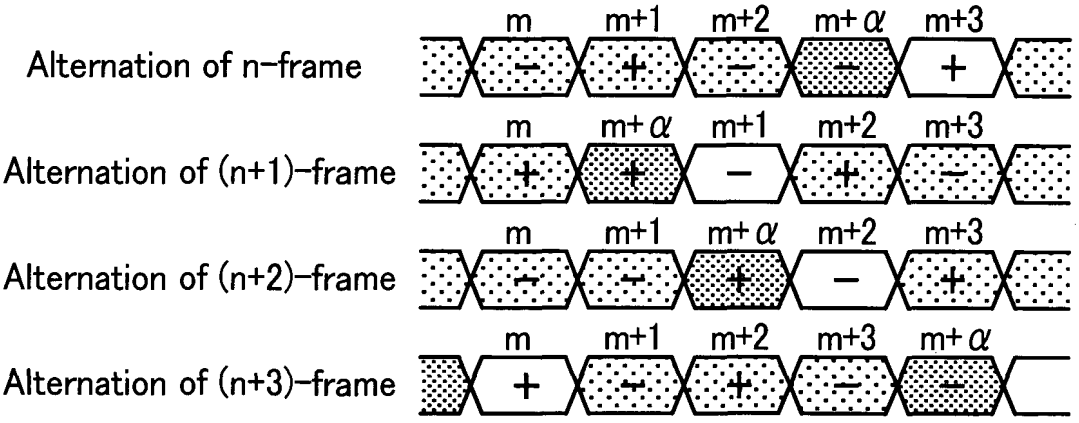


FIG. 32

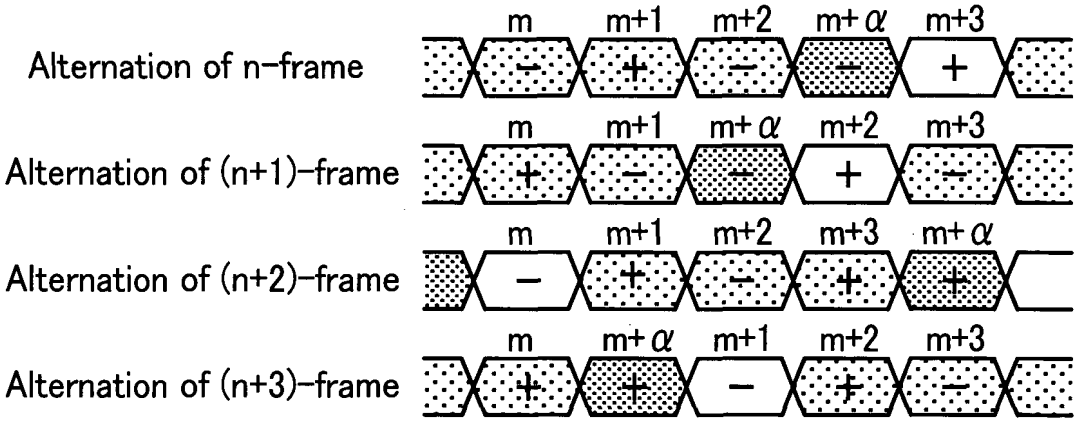

m
m+1
m+2
m+α
m+3
Alternation of n-frame
Alternation of (n+1)-frame
Alternation of (n+2)-frame
Alternation of (n+3)-frame

FIG. 33

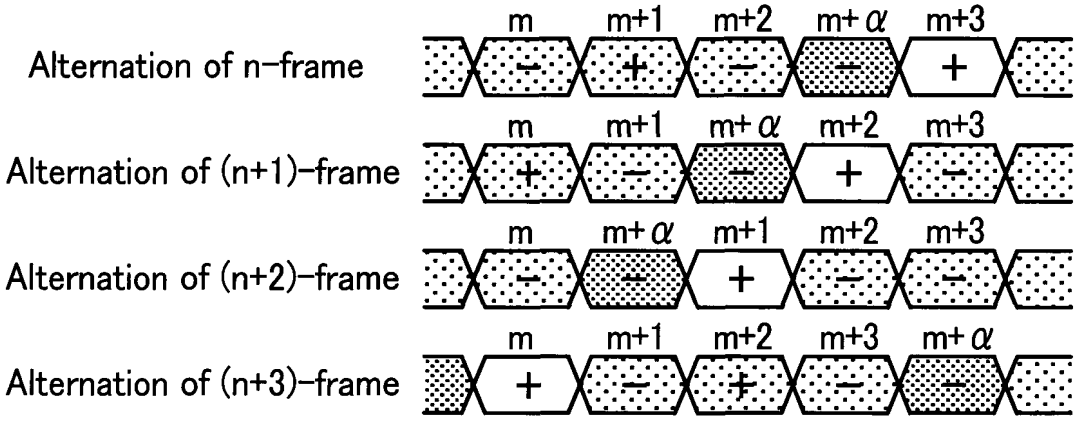

m
m+1
m+2
m+α
m+3
Alternation of n-frame
Alternation of (n+1)-frame
Alternation of (n+2)-frame
Alternation of (n+3)-frame

FIG. 34A

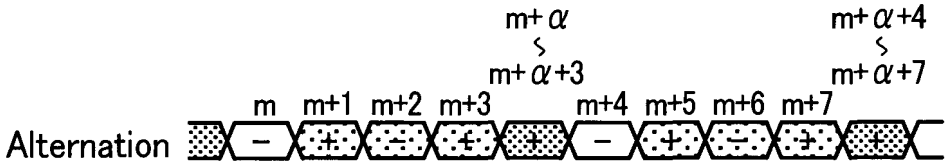


FIG. 34B

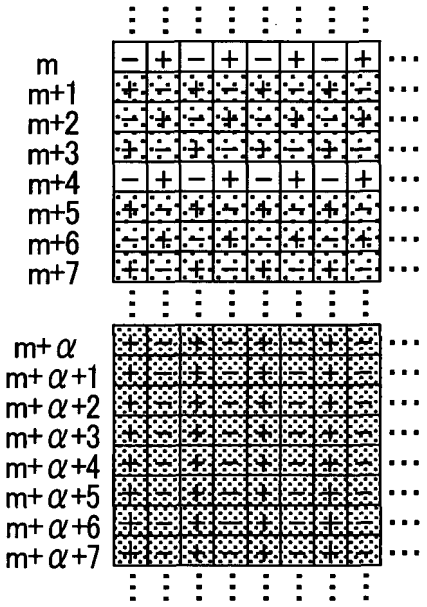


FIG. 34C

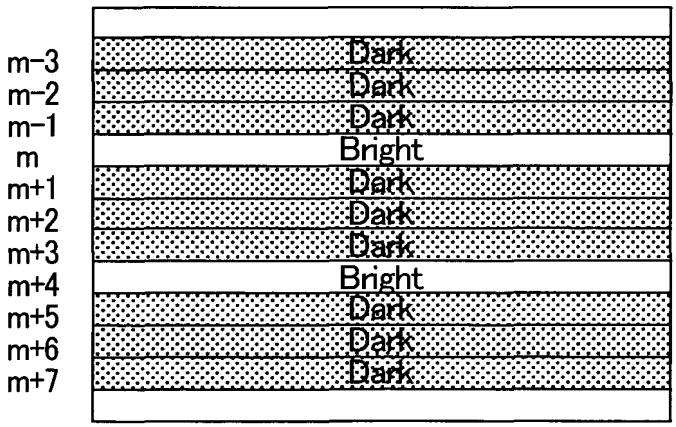


FIG. 35

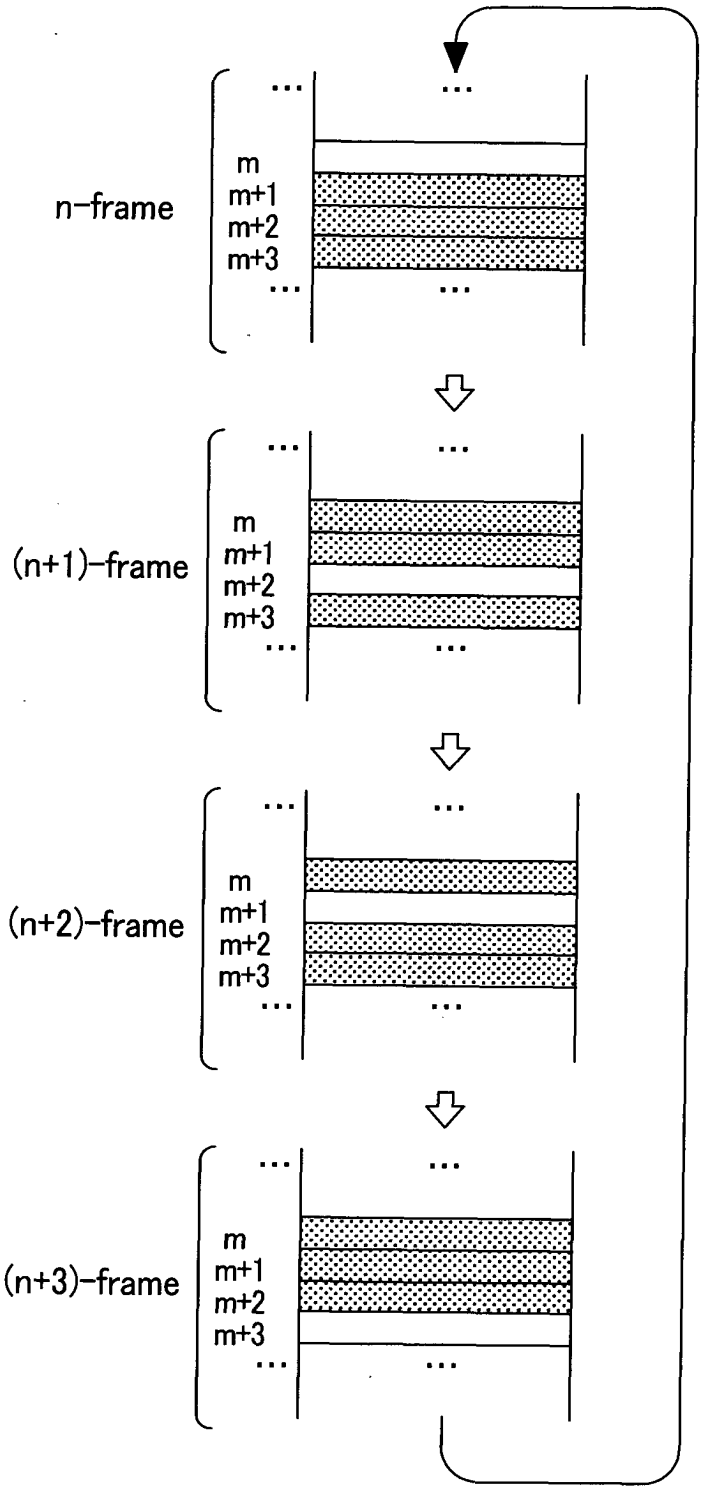

n-frame
m
m+1
m+2
m+3
(n+1)-frame
m
m+1
m+2
m+3
(n+2)-frame
m
m+1
m+2
m+3
(n+3)-frame
m
m+1
m+2
m+3

FIG. 36A

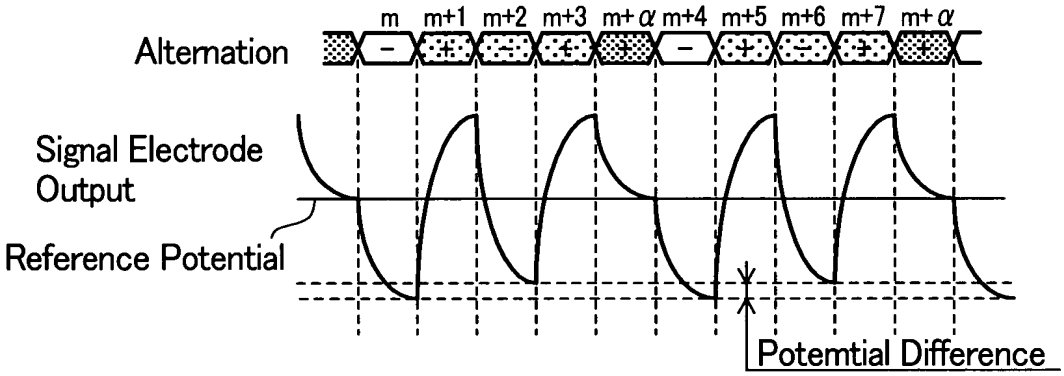


FIG. 36B

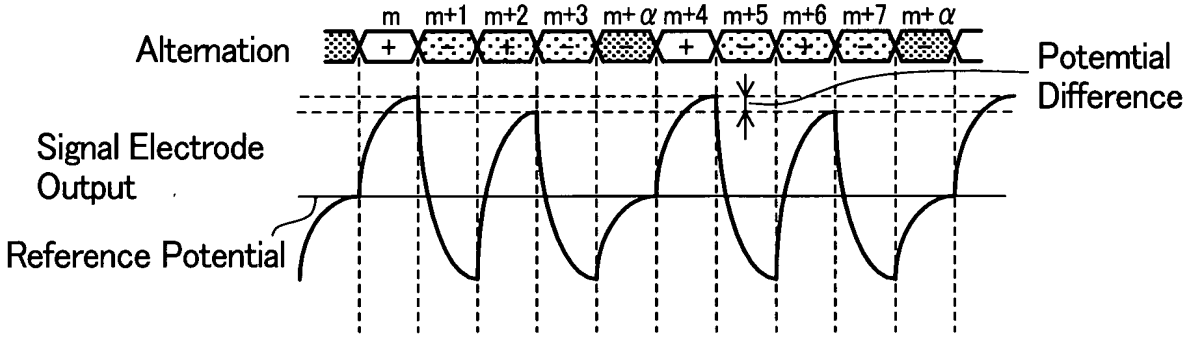


FIG. 37A

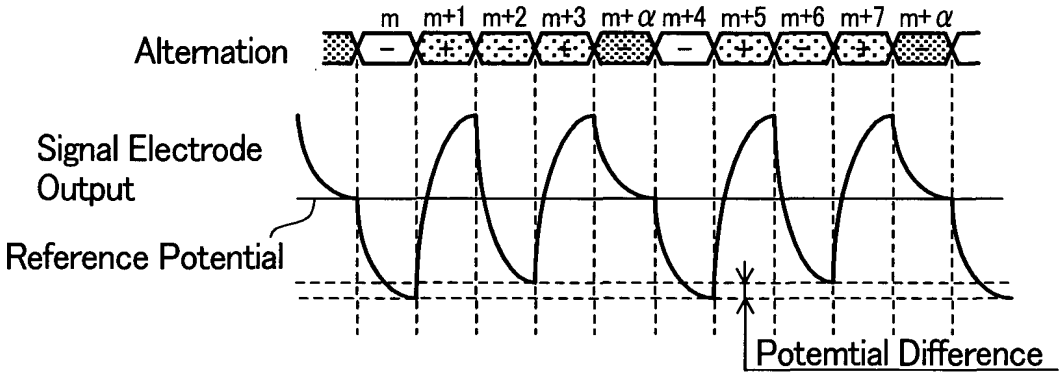


FIG. 37B

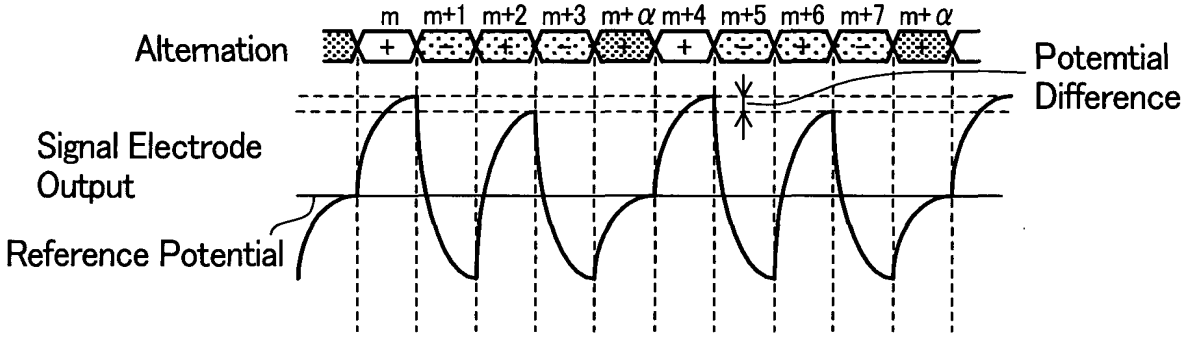


FIG. 38A

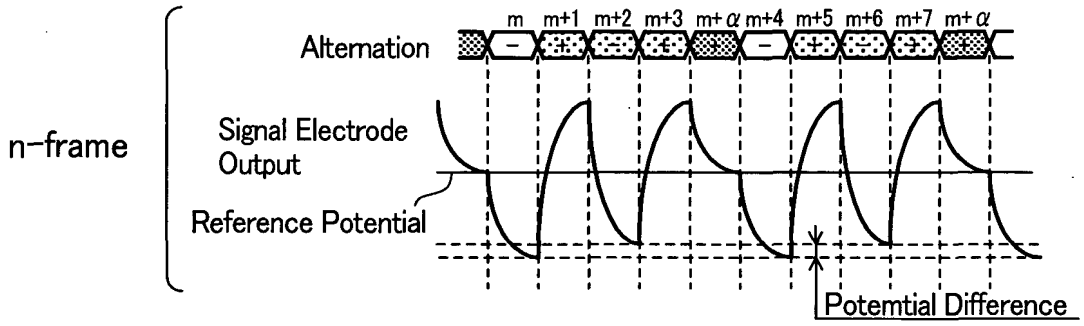


FIG. 38B

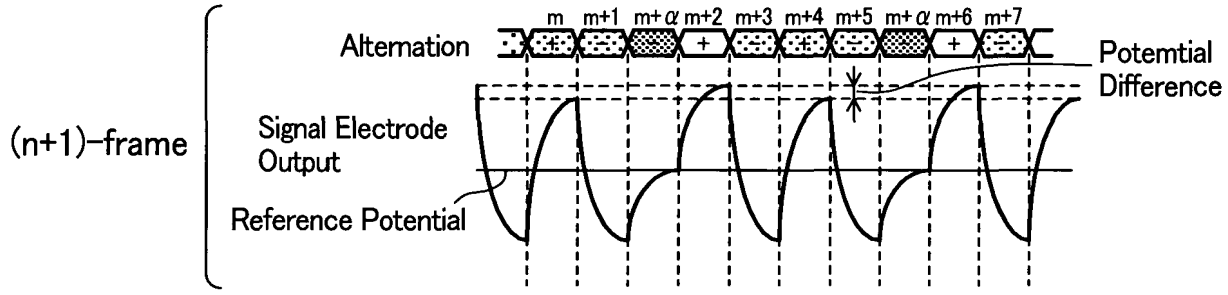


FIG. 38C

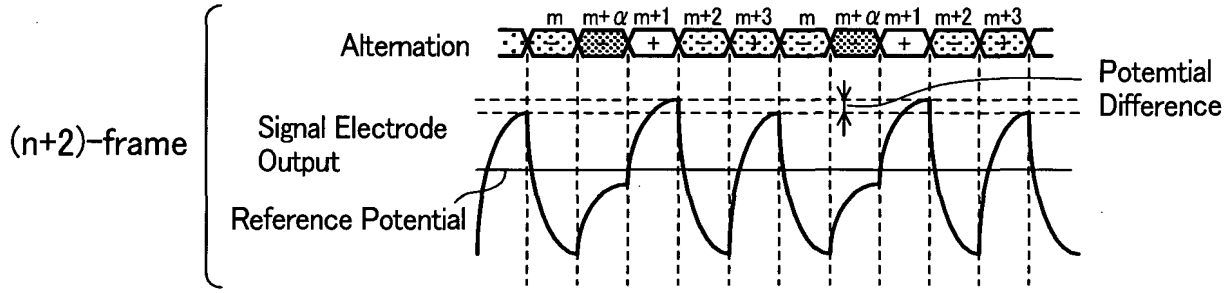


FIG. 38D

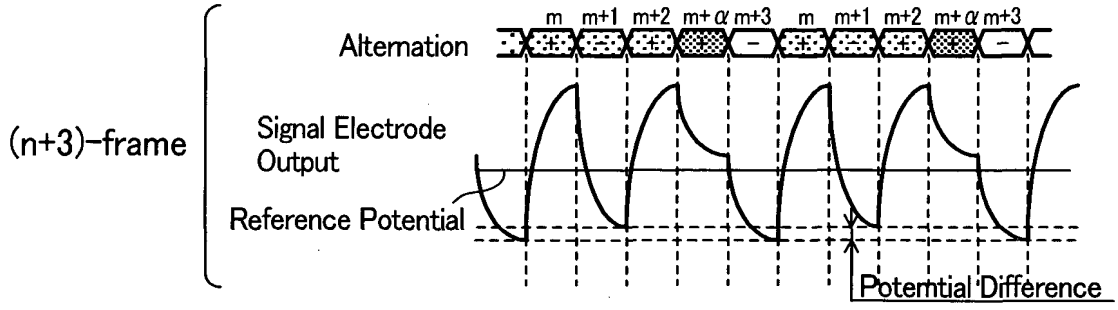


FIG. 39

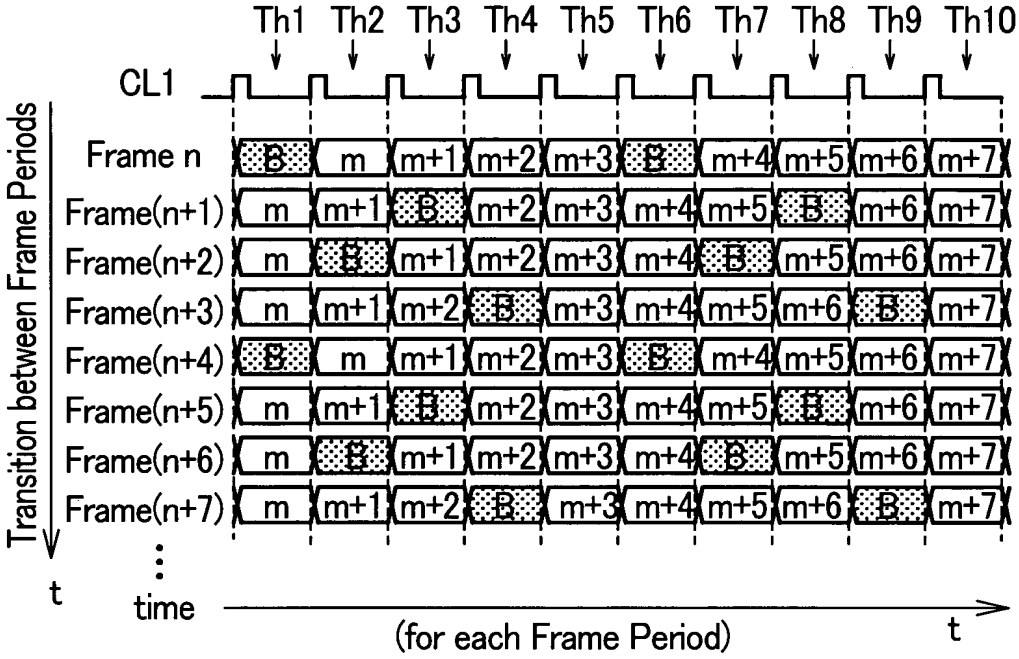

Th1 Th2 Th3 Th4 Th5 Th6 Th7 Th8 Th9 Th10
CL1
Frame n
Frame(n+1)
Frame(n+2)
Frame(n+3)
Frame(n+4)
Frame(n+5)
Frame(n+6)
Frame(n+7)
B
m
m+1
m+2
m+3
m+4
m+5
m+6
m+7
Transition between Frame Periods
t
time
(for each Frame Period)
t

FIG. 40

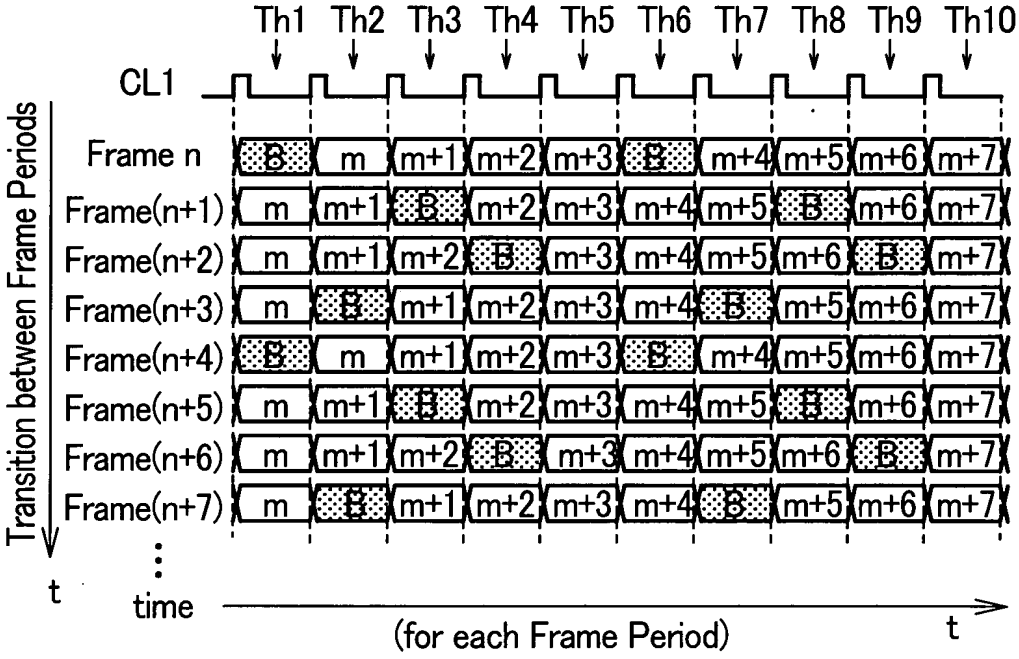

Th1 Th2 Th3 Th4 Th5 Th6 Th7 Th8 Th9 Th10
CL1
Frame n
Frame(n+1)
Frame(n+2)
Frame(n+3)
Frame(n+4)
Frame(n+5)
Frame(n+6)
Frame(n+7)
B
m
m+1
m+2
m+3
m+4
m+5
m+6
m+7
Transition between Frame Periods
t
time
(for each Frame Period)
t

FIG. 41

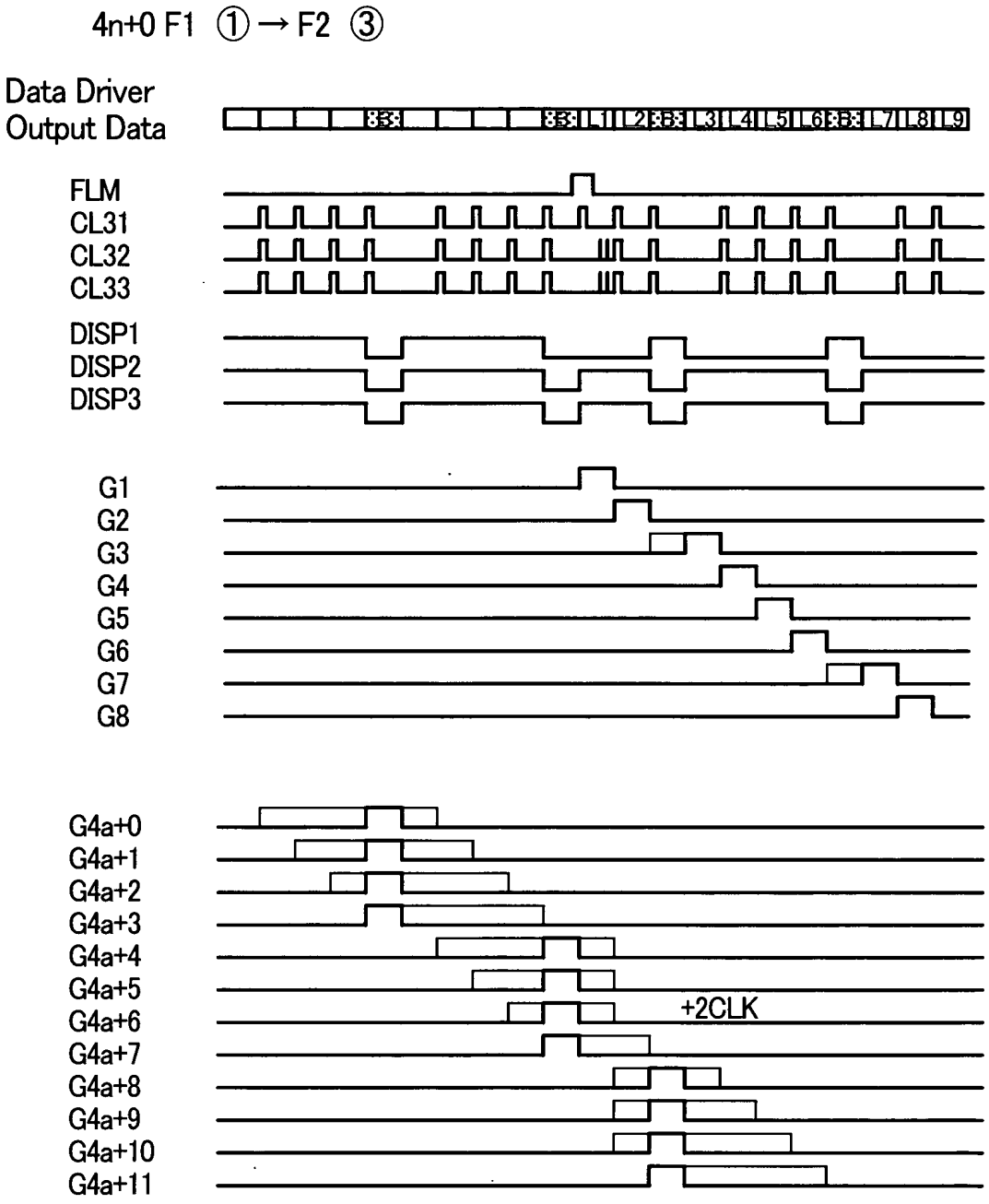

4n+0 F1 ① → F2 ③
Data Driver Output Data
FLM
CL31
CL32
CL33
DISP1
DISP2
DISP3
G1
G2
G3
G4
G5
G6
G7
G8
G4a+0
G4a+1
G4a+2
G4a+3
G4a+4
G4a+5
G4a+6
G4a+7
G4a+8
G4a+9
G4a+10
G4a+11
+2CLK

FIG. 42

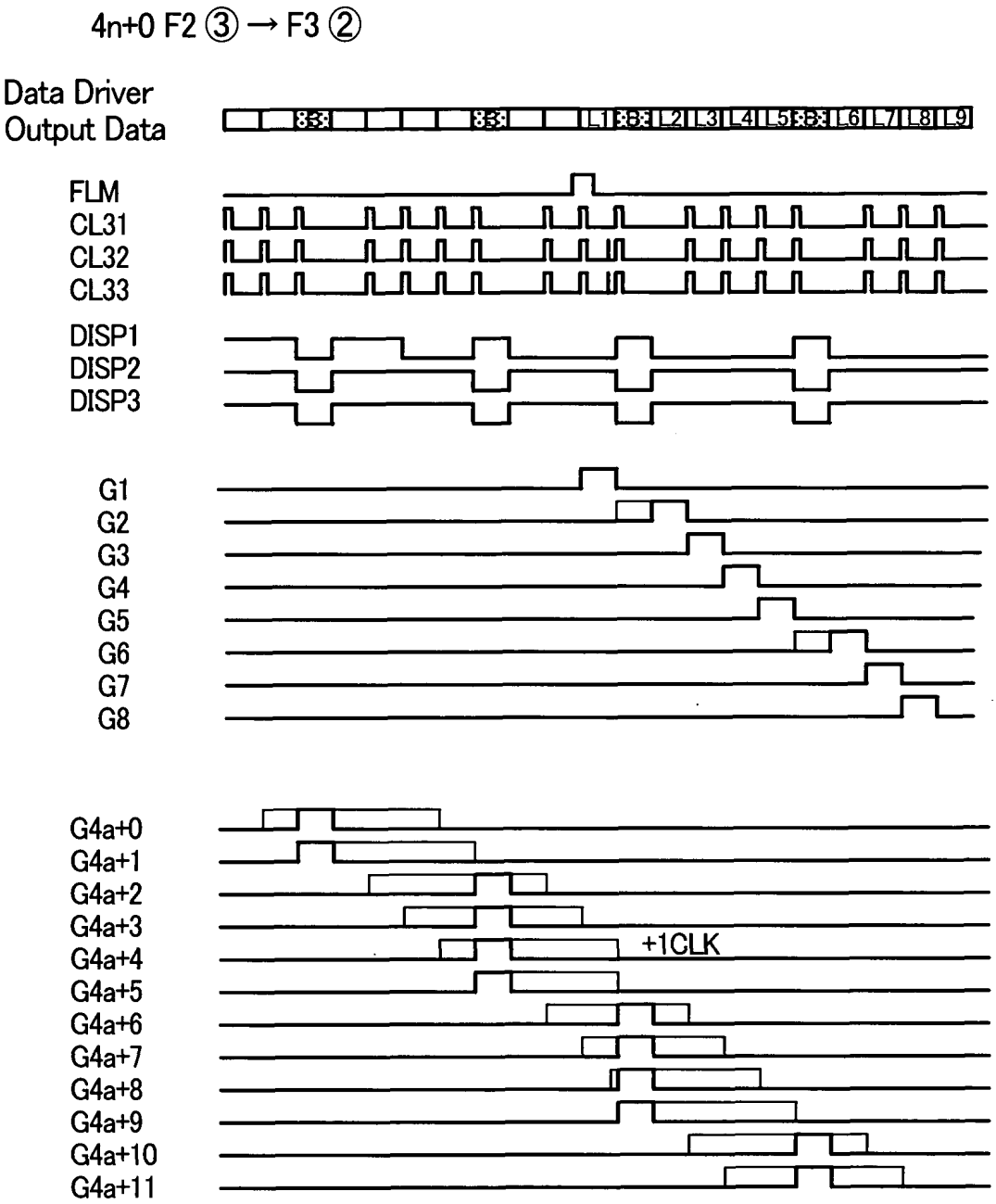

4n+0 F2 ③ → F3 ②
Data Driver Output Data
L1
L2
L3
L4
L5
L6
L7
L8
L9
FLM
CL31
CL32
CL33
DISP1
DISP2
DISP3
G1
G2
G3
G4
G5
G6
G7
G8
G4a+0
G4a+1
G4a+2
G4a+3
G4a+4
G4a+5
G4a+6
G4a+7
G4a+8
G4a+9
G4a+10
G4a+11
+1CLK

FIG. 43

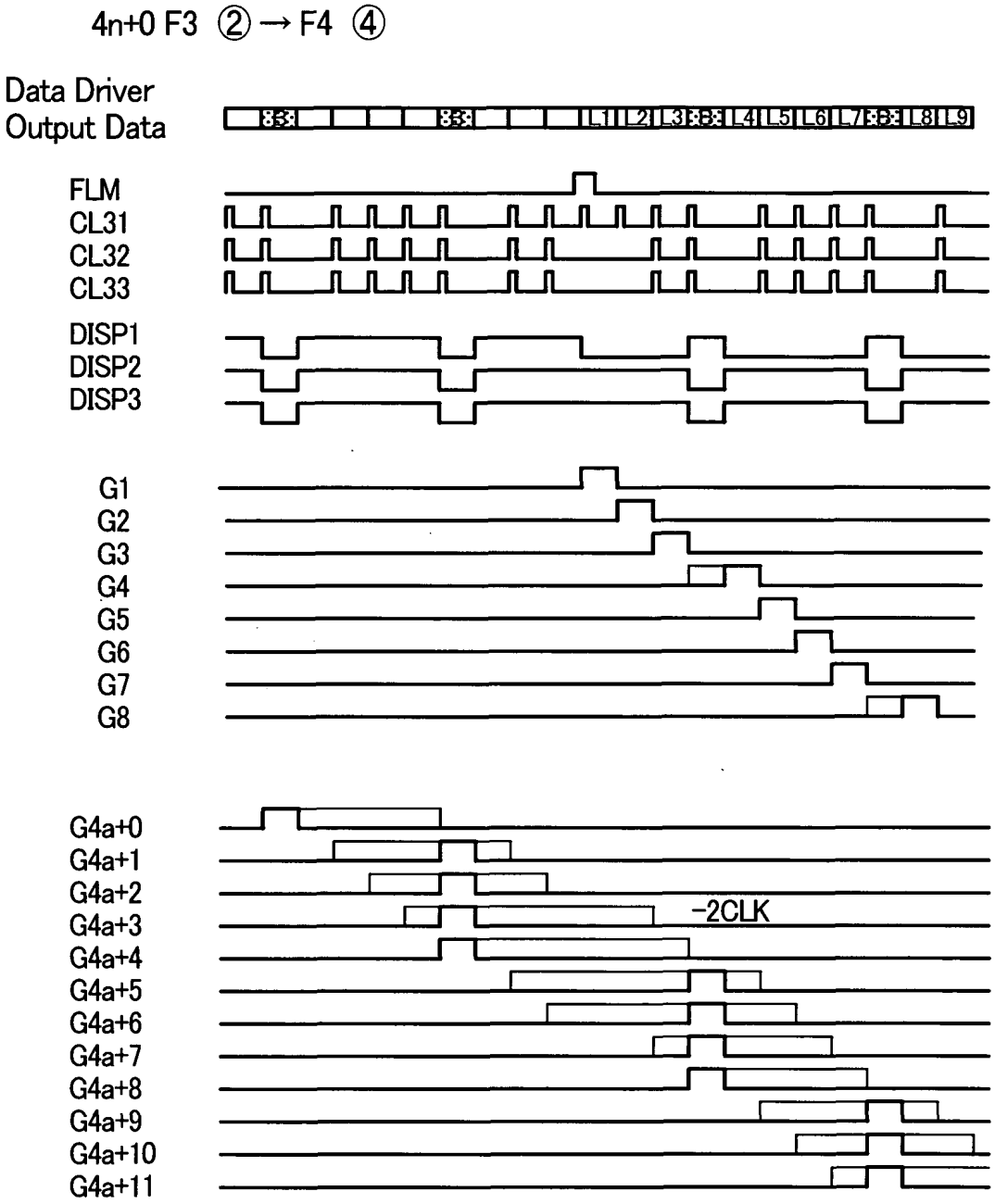

4n+0 F3 ② → F4 ④
Data Driver Output Data
L1
L2
L3
L4
L5
L6
L7
L8
L9
FLM
CL31
CL32
CL33
DISP1
DISP2
DISP3
G1
G2
G3
G4
G5
G6
G7
G8
G4a+0
G4a+1
G4a+2
G4a+3
G4a+4
G4a+5
G4a+6
G4a+7
G4a+8
G4a+9
G4a+10
G4a+11
-2CLK

FIG 44

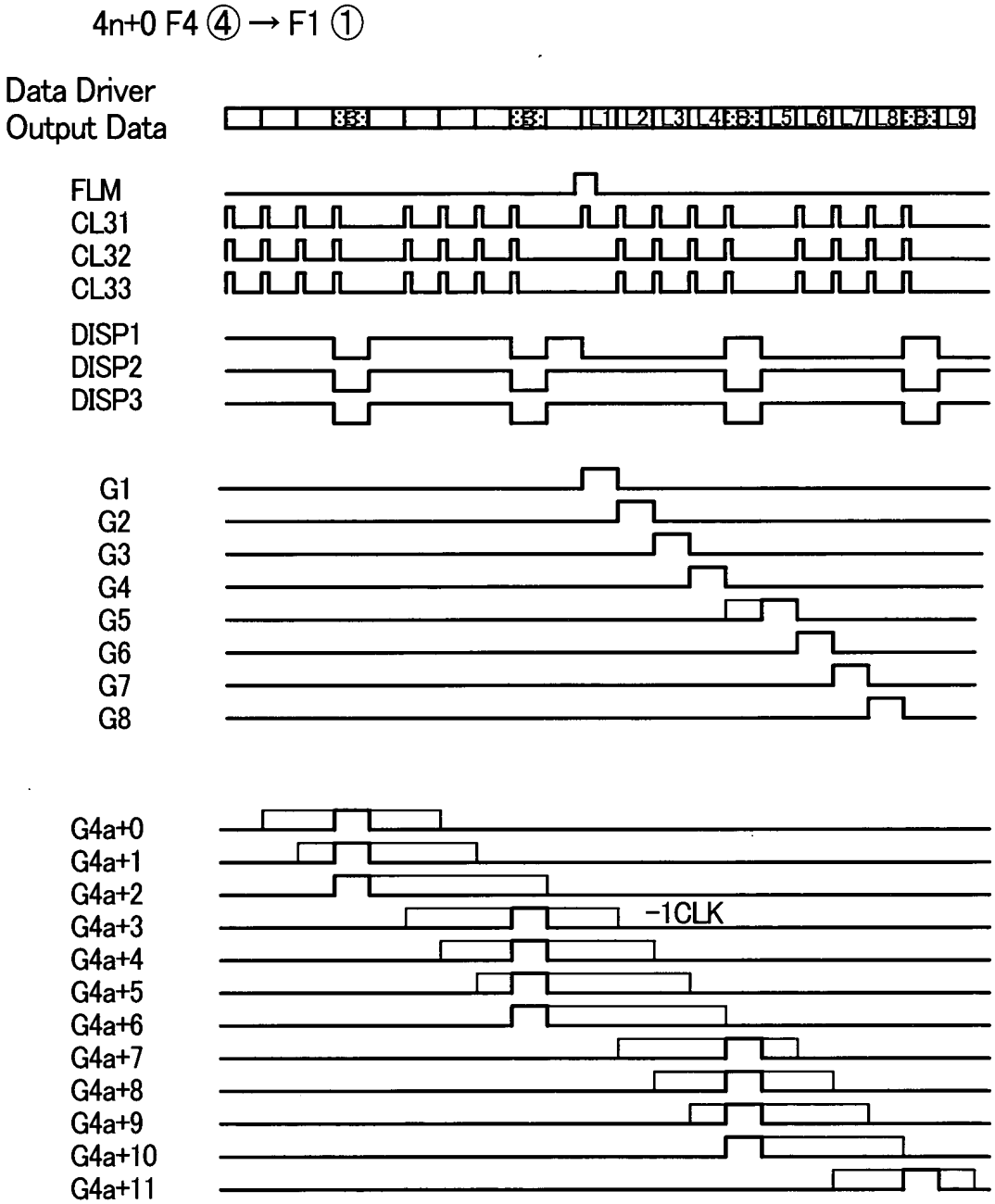

4n+0 F4 ④ → F1 ①
Data Driver Output Data
L1
L2
L3
L4
L5
L6
L7
L8
L9
FLM
CL31
CL32
CL33
DISP1
DISP2
DISP3
G1
G2
G3
G4
G5
G6
G7
G8
G4a+0
G4a+1
G4a+2
G4a+3
G4a+4
G4a+5
G4a+6
G4a+7
G4a+8
G4a+9
G4a+10
G4a+11
-1CLK

FIG. 45

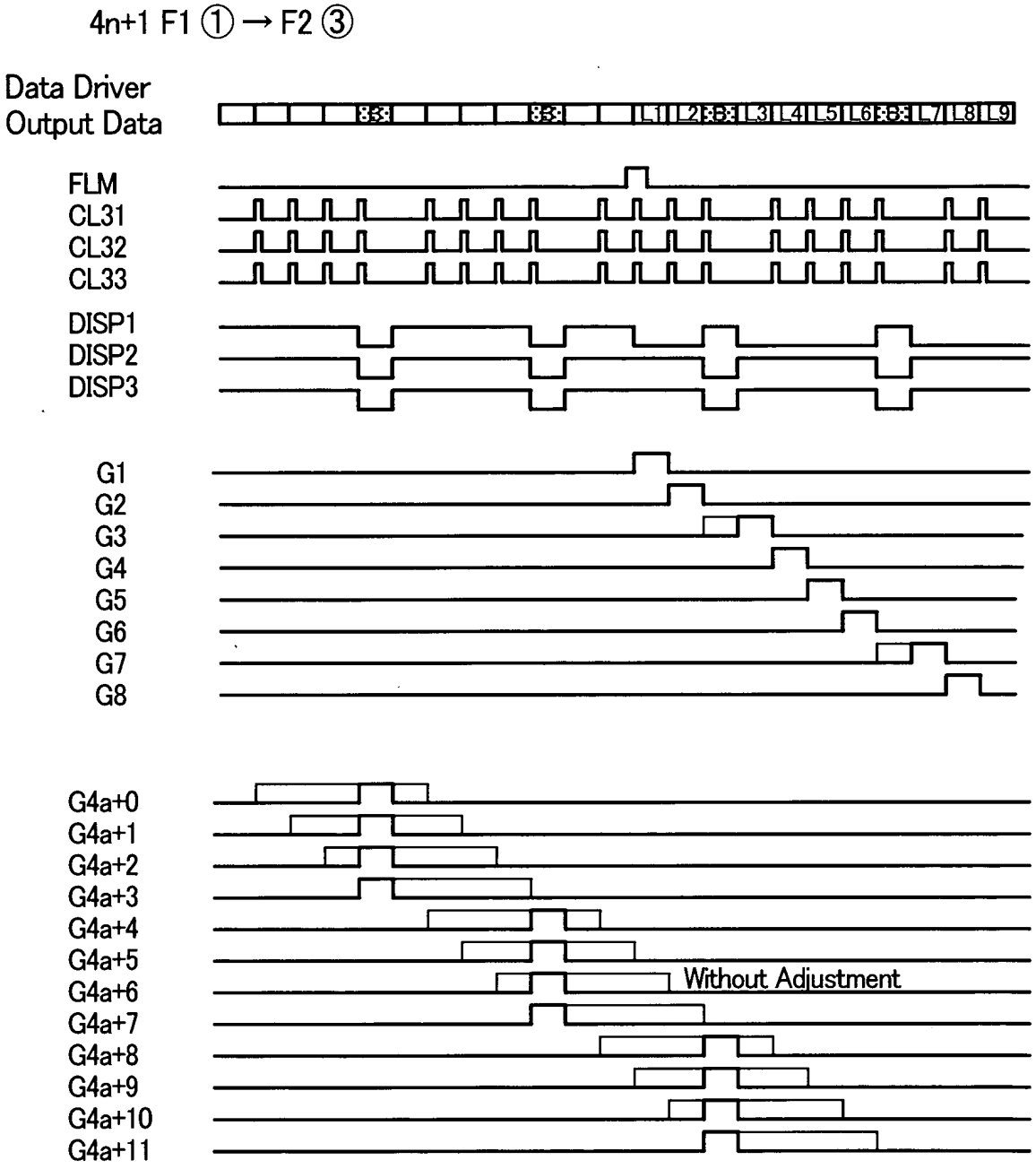

4n+1 F1 ① → F2 ③
Data Driver Output Data
L1
L2
L3
L4
L5
L6
L7
L8
L9
FLM
CL31
CL32
CL33
DISP1
DISP2
DISP3
G1
G2
G3
G4
G5
G6
G7
G8
G4a+0
G4a+1
G4a+2
G4a+3
G4a+4
G4a+5
G4a+6
G4a+7
G4a+8
G4a+9
G4a+10
G4a+11
Without Adjustment

FIG. 46

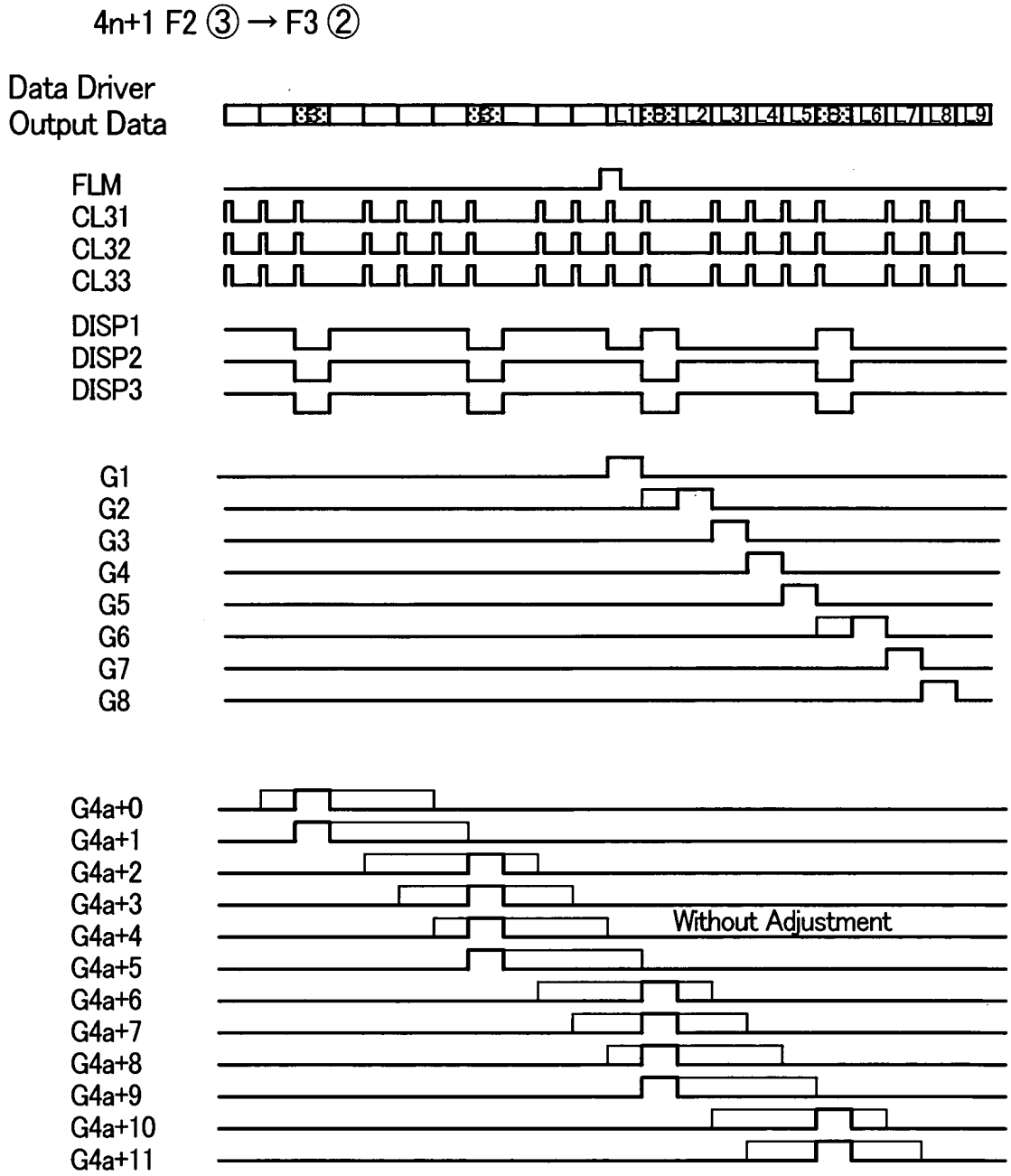

4n+1 F2 ③ → F3 ②
Data Driver Output Data
L1
L2
L3
L4
L5
L6
L7
L8
L9
FLM
CL31
CL32
CL33
DISP1
DISP2
DISP3
G1
G2
G3
G4
G5
G6
G7
G8
G4a+0
G4a+1
G4a+2
G4a+3
G4a+4
G4a+5
G4a+6
G4a+7
G4a+8
G4a+9
G4a+10
G4a+11
Without Adjustment

FIG. 47

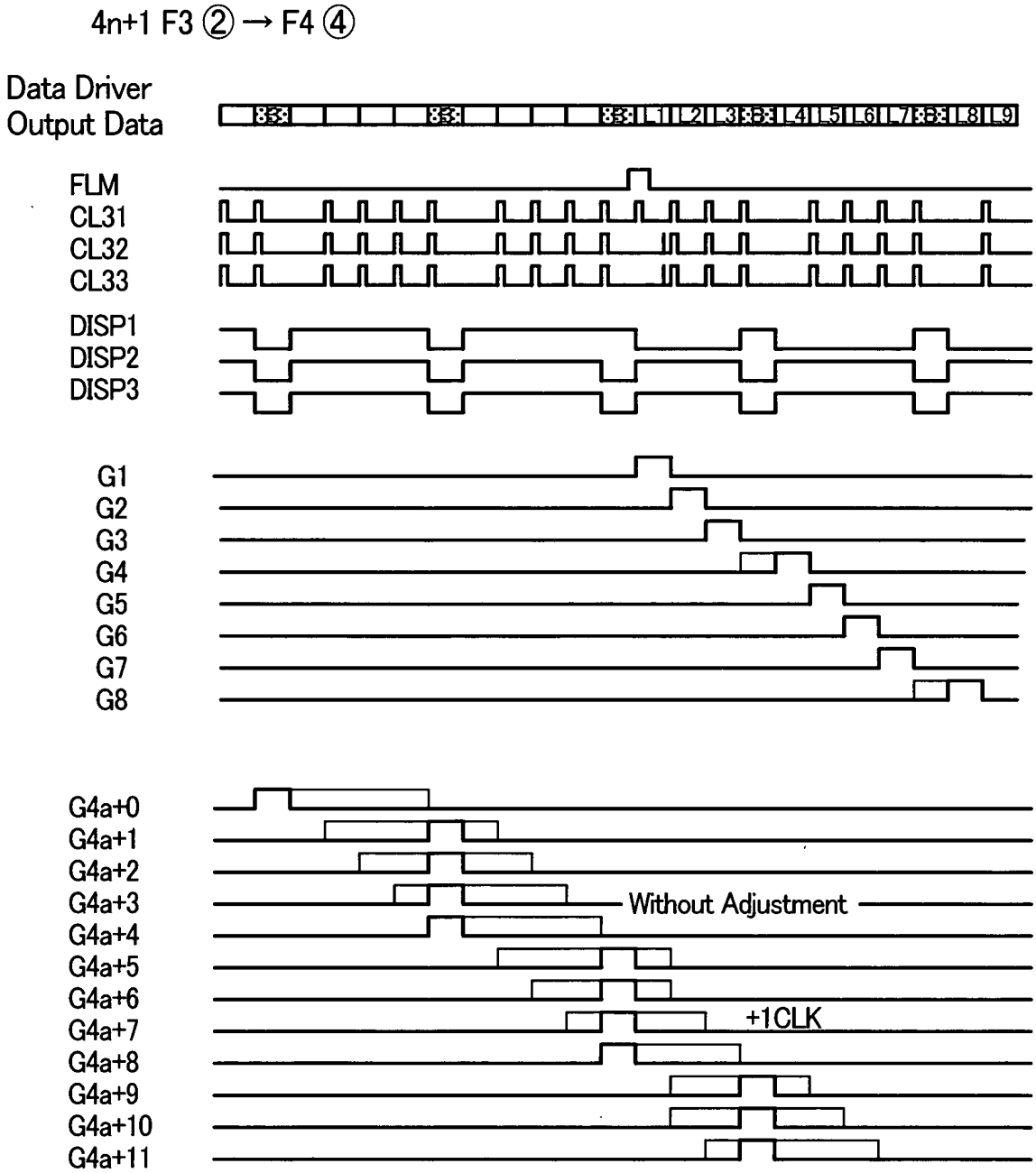

4n+1 F3 ② → F4 ④
Data Driver Output Data
L1
L2
L3
L4
L5
L6
L7
L8
L9
FLM
CL31
CL32
CL33
DISP1
DISP2
DISP3
G1
G2
G3
G4
G5
G6
G7
G8
G4a+0
G4a+1
G4a+2
G4a+3
G4a+4
G4a+5
G4a+6
G4a+7
G4a+8
G4a+9
G4a+10
G4a+11
Without Adjustment
+1CLK

FIG. 48

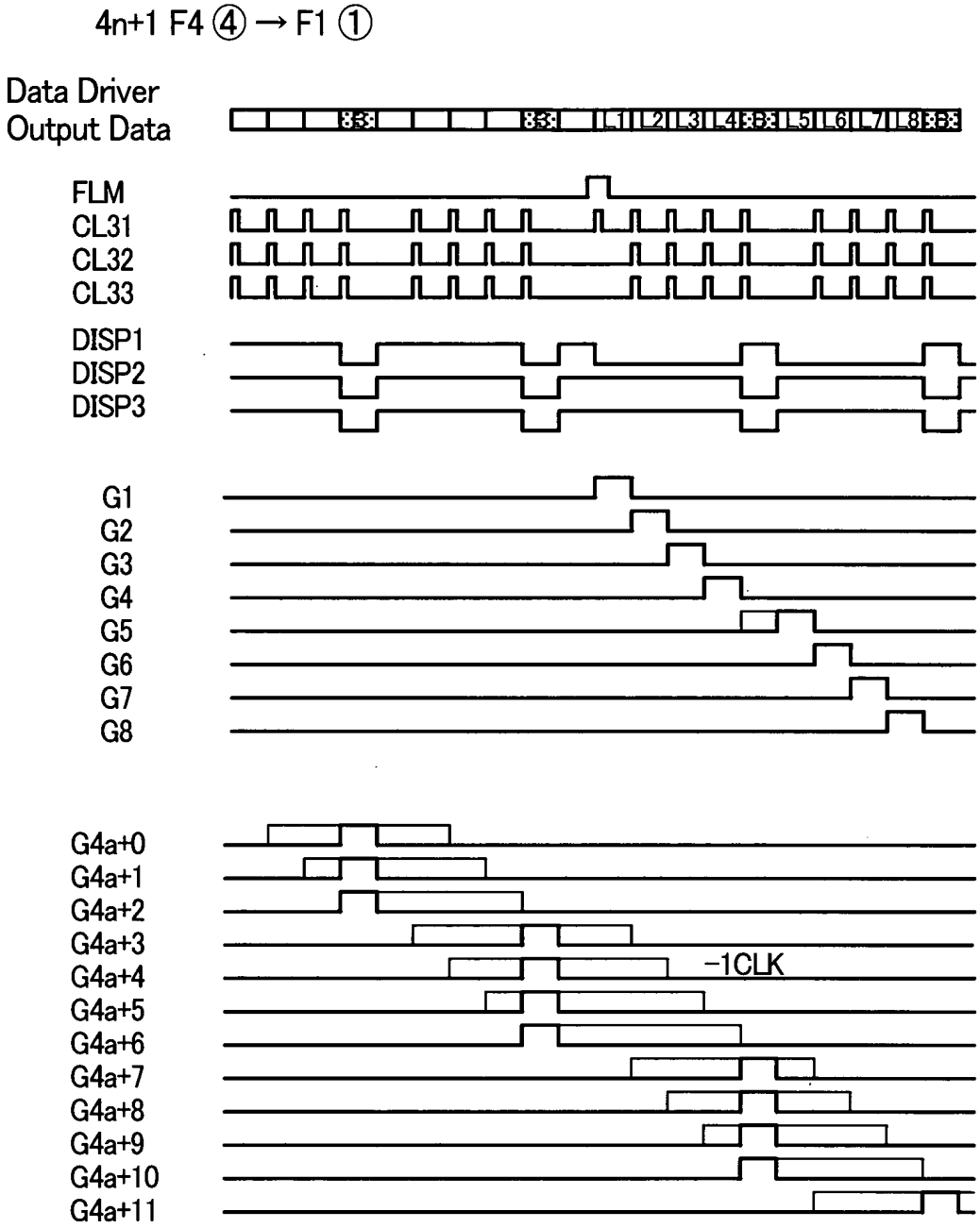

4n+1 F4 ④ → F1 ①
Data Driver Output Data
L1
L2
L3
L4
L5
L6
L7
L8
FLM
CL31
CL32
CL33
DISP1
DISP2
DISP3
G1
G2
G3
G4
G5
G6
G7
G8
G4a+0
G4a+1
G4a+2
G4a+3
G4a+4
G4a+5
G4a+6
G4a+7
G4a+8
G4a+9
G4a+10
G4a+11
-1CLK

FIG. 49

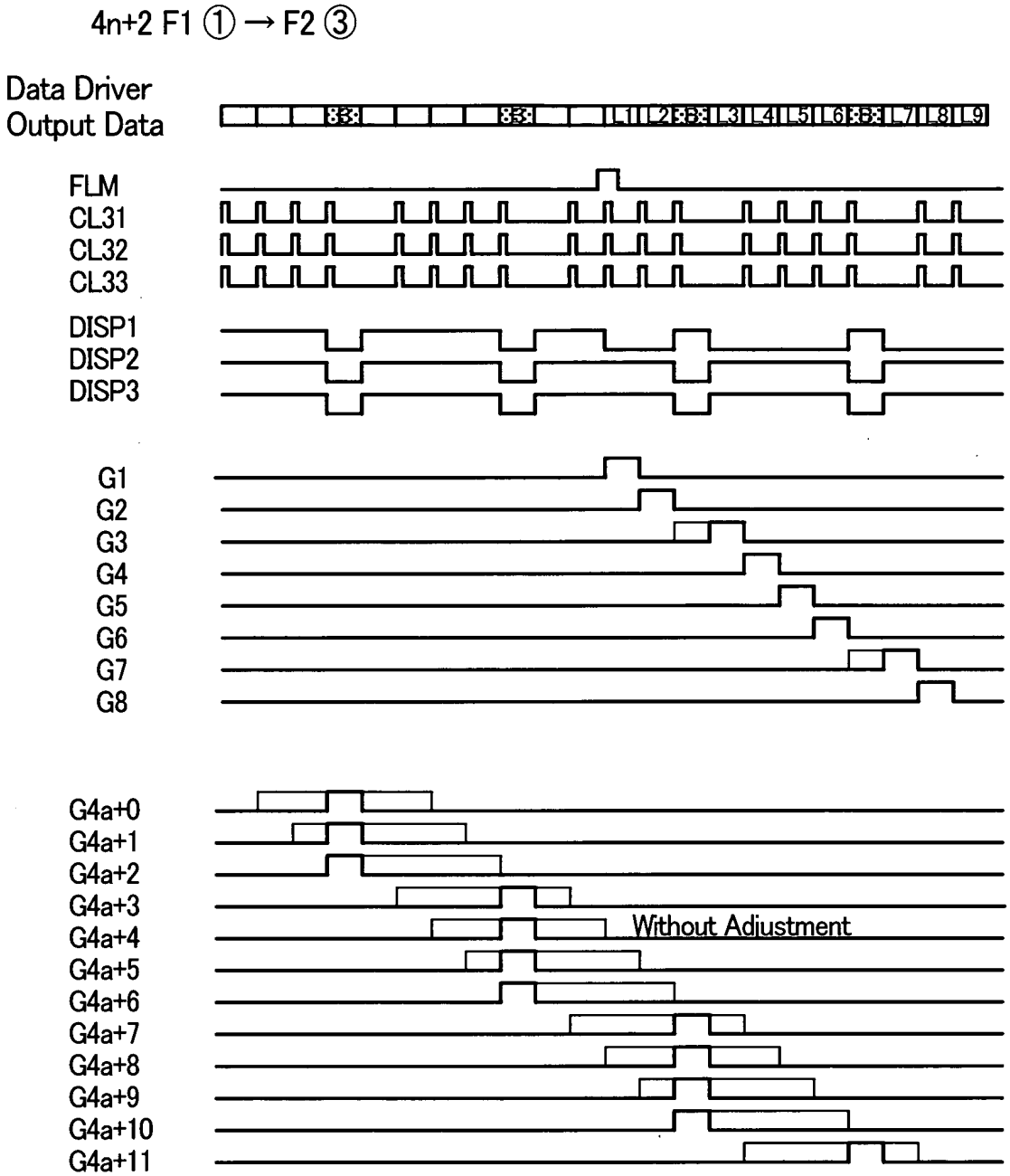

4n+2 F1 ① → F2 ③
Data Driver Output Data
L1
L2
L3
L4
L5
L6
L7
L8
L9
FLM
CL31
CL32
CL33
DISP1
DISP2
DISP3
G1
G2
G3
G4
G5
G6
G7
G8
G4a+0
G4a+1
G4a+2
G4a+3
G4a+4
G4a+5
G4a+6
G4a+7
G4a+8
G4a+9
G4a+10
G4a+11
Without Adjustment

FIG. 50

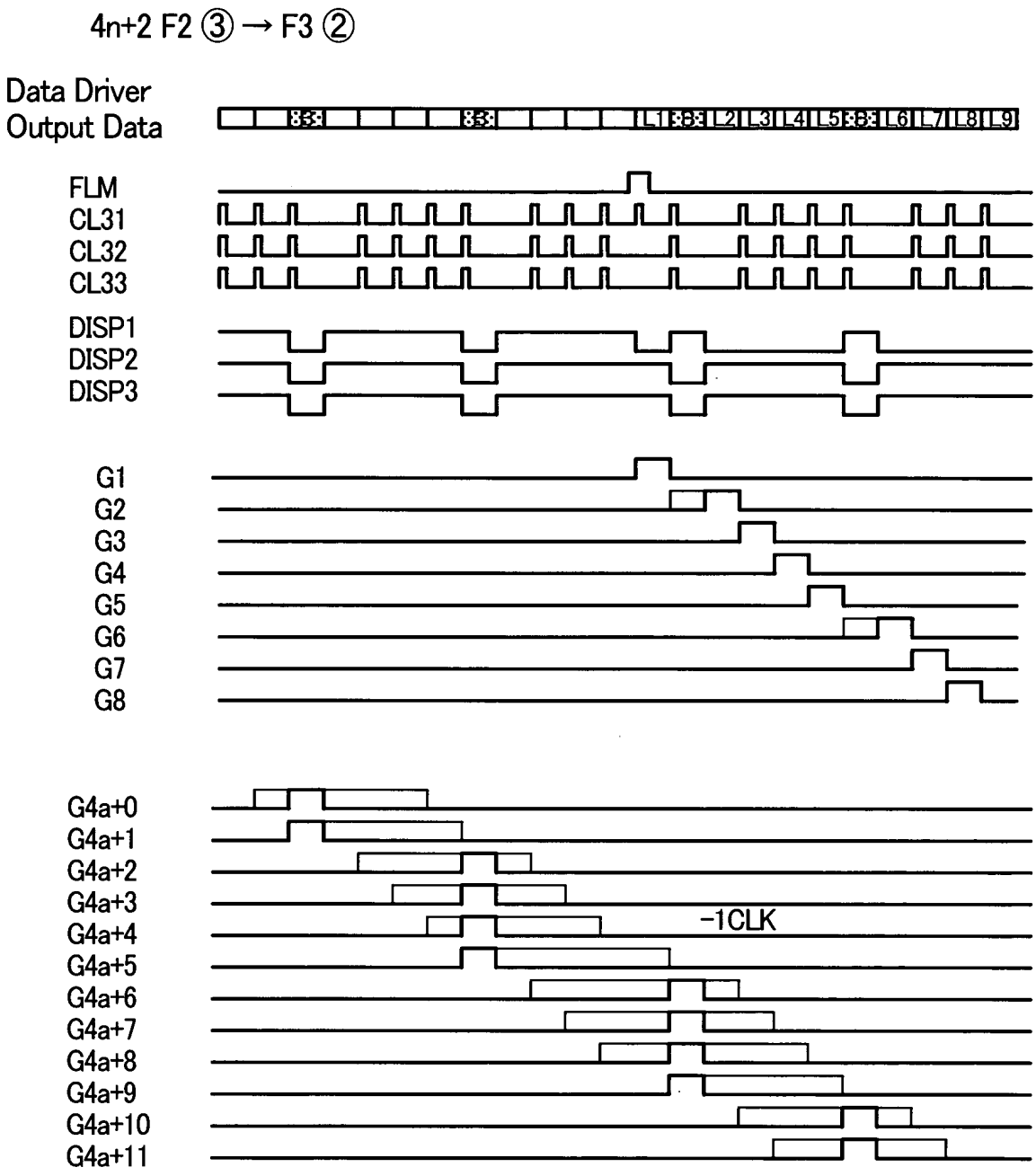

4n+2 F2 ③ → F3 ②
Data Driver Output Data
L1
L2
L3
L4
L5
L6
L7
L8
L9
FLM
CL31
CL32
CL33
DISP1
DISP2
DISP3
G1
G2
G3
G4
G5
G6
G7
G8
G4a+0
G4a+1
G4a+2
G4a+3
G4a+4
G4a+5
G4a+6
G4a+7
G4a+8
G4a+9
G4a+10
G4a+11
-1CLK

FIG. 51

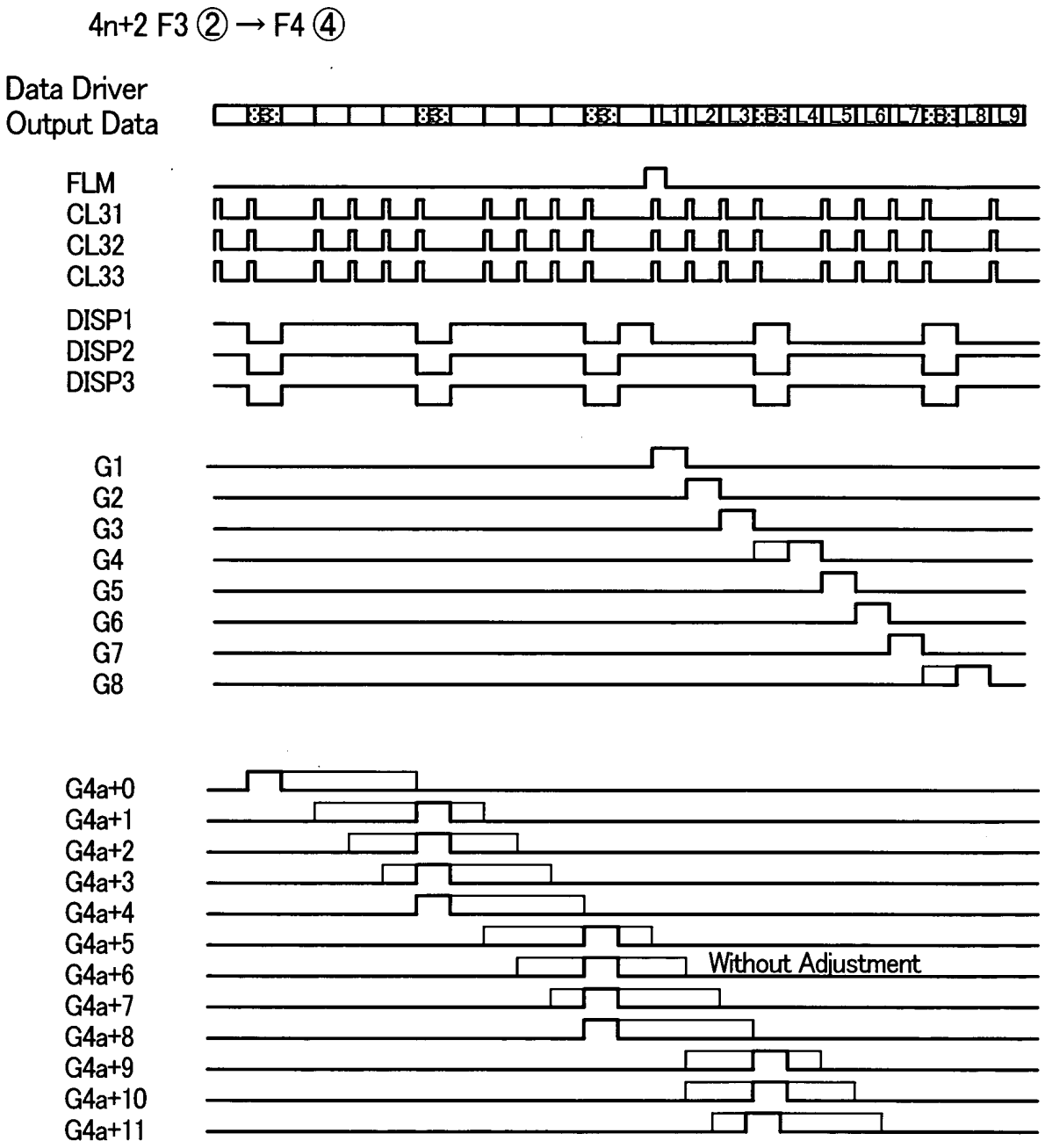

4n+2 F3 ② → F4 ④
Data Driver Output Data
L1
L2
L3
L4
L5
L6
L7
L8
L9
FLM
CL31
CL32
CL33
DISP1
DISP2
DISP3
G1
G2
G3
G4
G5
G6
G7
G8
G4a+0
G4a+1
G4a+2
G4a+3
G4a+4
G4a+5
G4a+6
G4a+7
G4a+8
G4a+9
G4a+10
G4a+11
Without Adjustment

FIG. 52

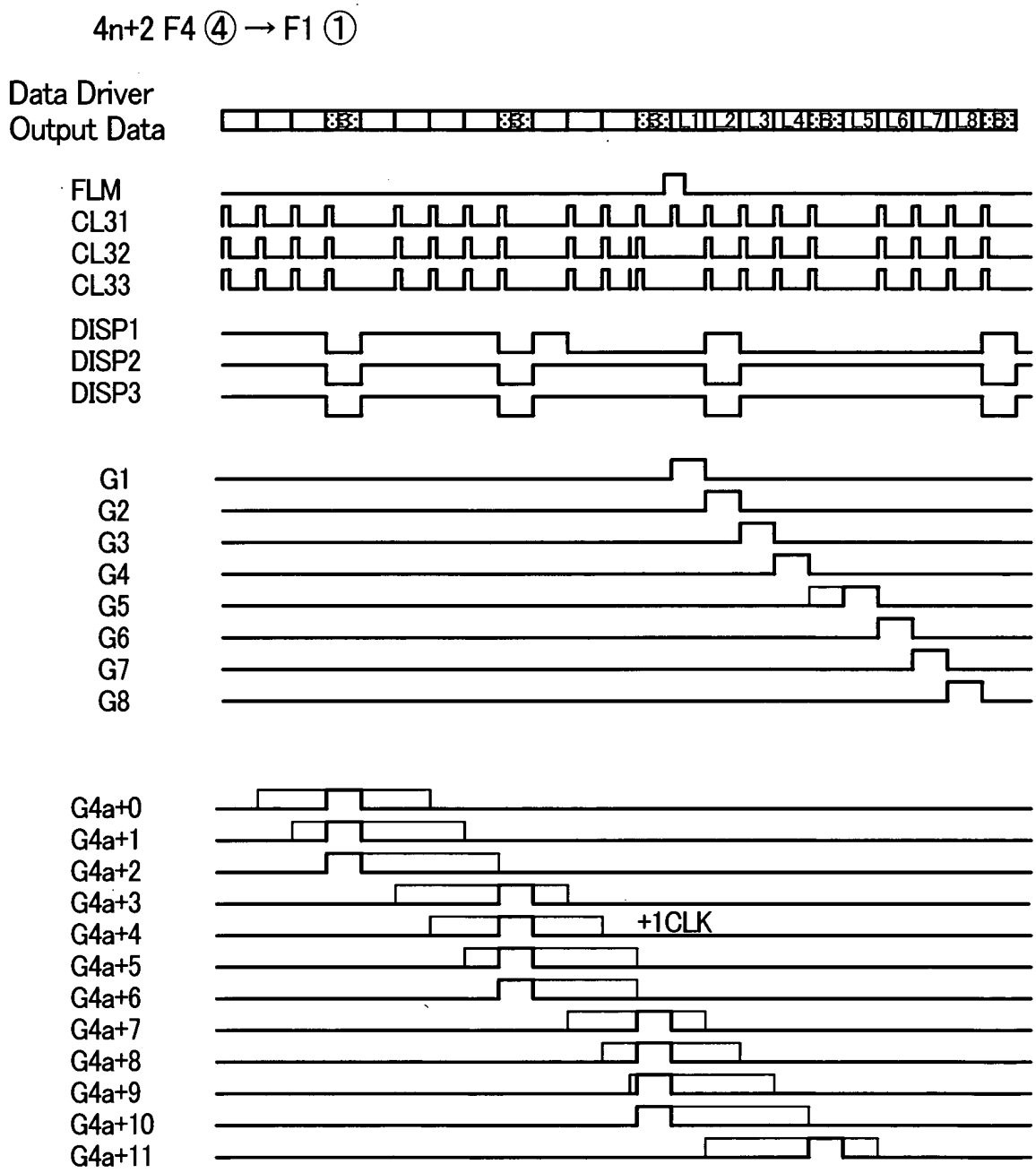

4n+2 F4 ④ → F1 ①
Data Driver Output Data
FLM
CL31
CL32
CL33
DISP1
DISP2
DISP3
G1
G2
G3
G4
G5
G6
G7
G8
G4a+0
G4a+1
G4a+2
G4a+3
G4a+4
G4a+5
G4a+6
G4a+7
G4a+8
G4a+9
G4a+10
G4a+11
+1CLK

FIG. 53

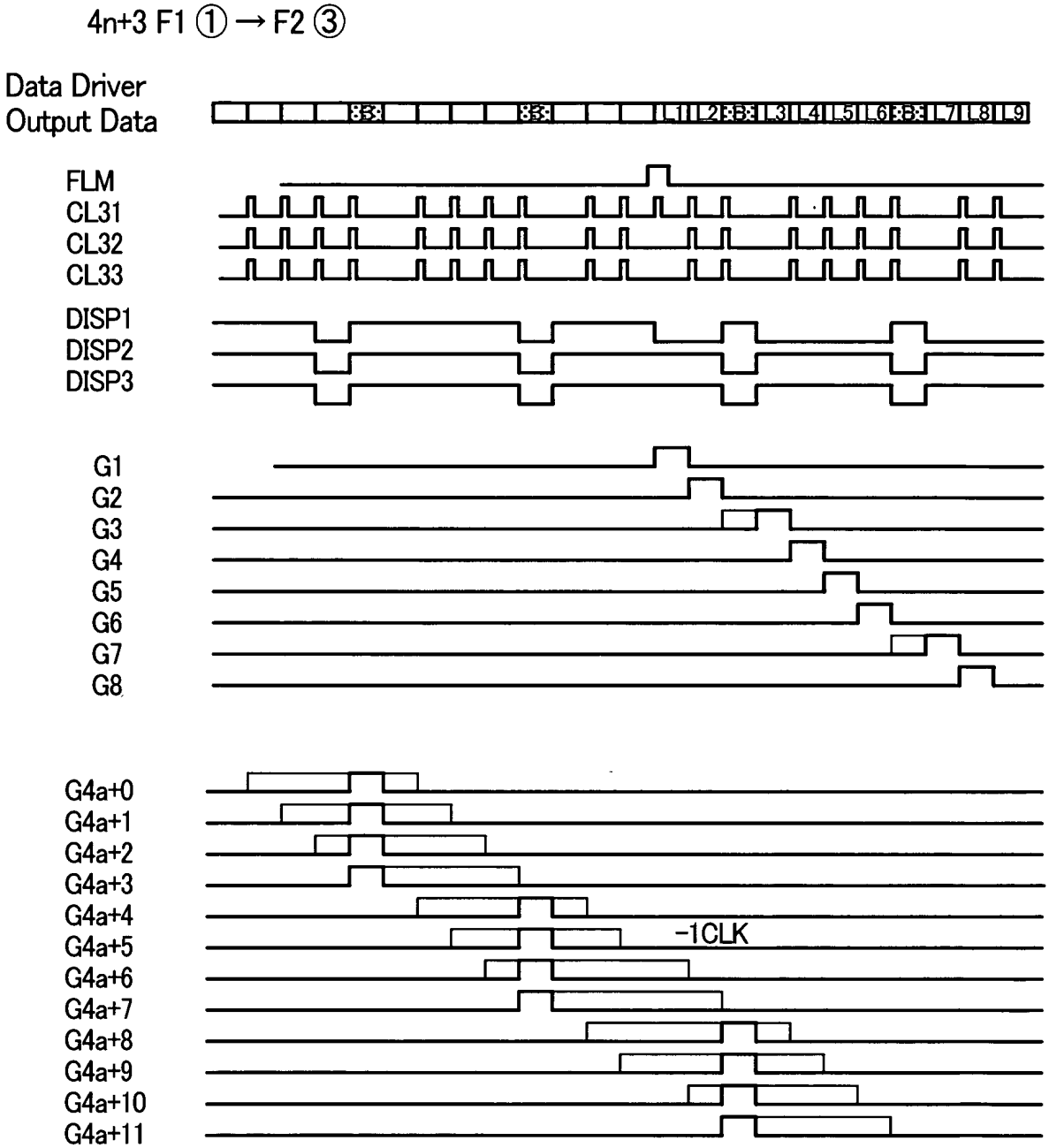

4n+3 F1 ① → F2 ③
Data Driver Output Data
L1
L2
L3
L4
L5
L6
L7
L8
L9
FLM
CL31
CL32
CL33
DISP1
DISP2
DISP3
G1
G2
G3
G4
G5
G6
G7
G8
G4a+0
G4a+1
G4a+2
G4a+3
G4a+4
G4a+5
G4a+6
G4a+7
G4a+8
G4a+9
G4a+10
G4a+11
-1CLK

FIG. 54

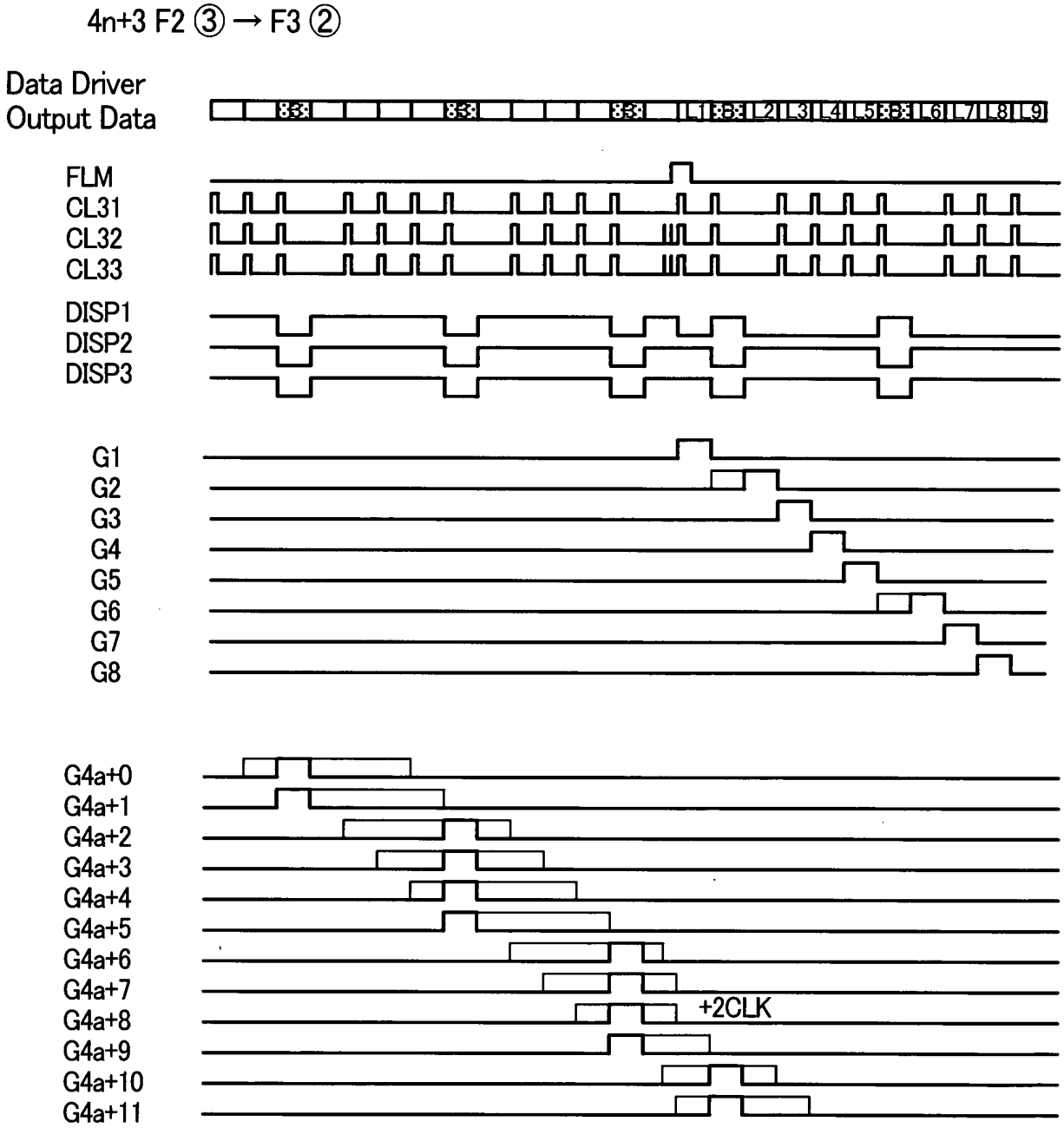

4n+3 F2 ③ → F3 ②
Data Driver Output Data
L1
L2
L3
L4
L5
L6
L7
L8
L9
FLM
CL31
CL32
CL33
DISP1
DISP2
DISP3
G1
G2
G3
G4
G5
G6
G7
G8
G4a+0
G4a+1
G4a+2
G4a+3
G4a+4
G4a+5
G4a+6
G4a+7
G4a+8
G4a+9
G4a+10
G4a+11
+2CLK

FIG. 55

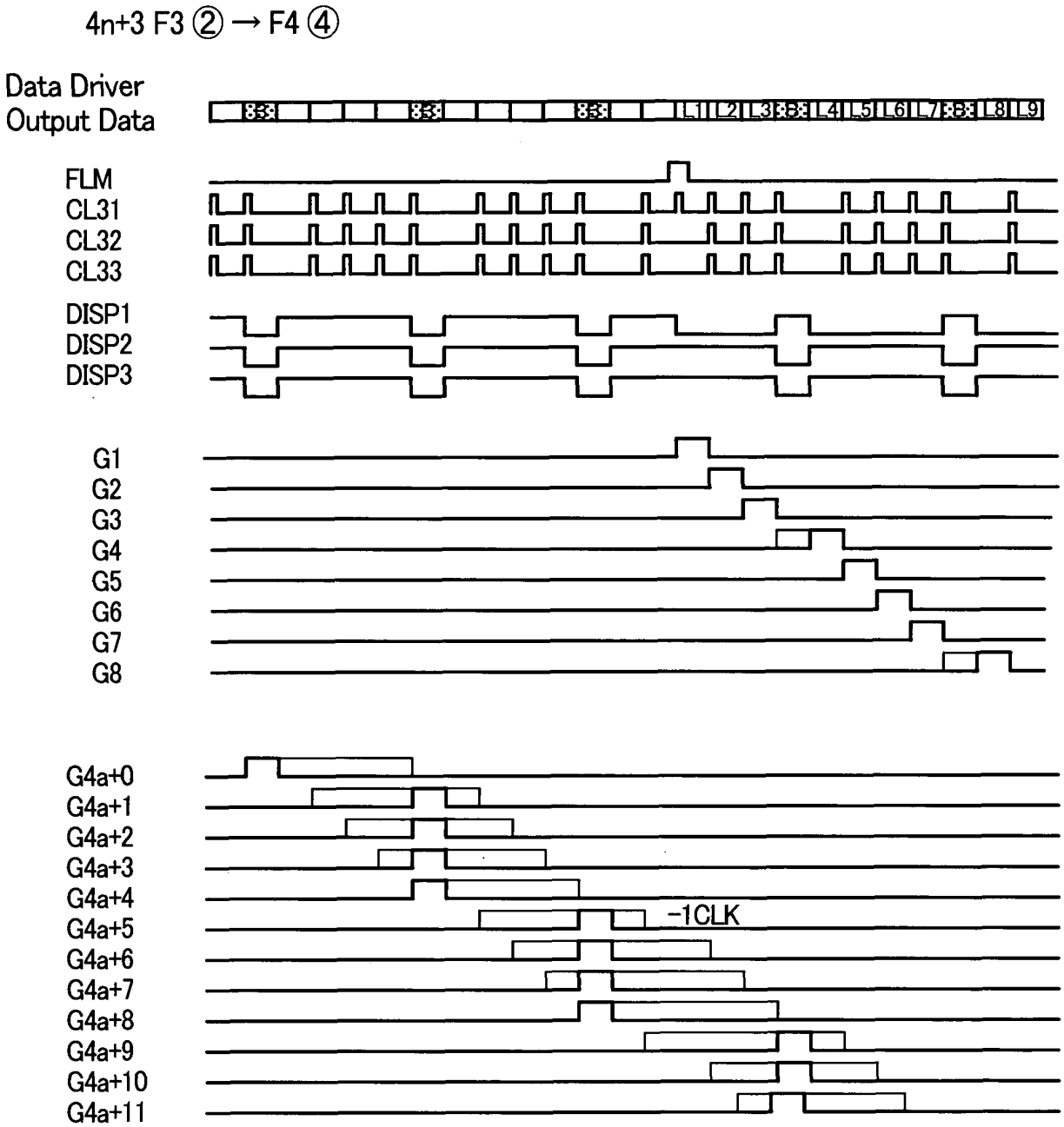

4n+3 F3 ② → F4 ④
Data Driver Output Data
L1
L2
L3
L4
L5
L6
L7
L8
L9
FLM
CL31
CL32
CL33
DISP1
DISP2
DISP3
G1
G2
G3
G4
G5
G6
G7
G8
G4a+0
G4a+1
G4a+2
G4a+3
G4a+4
G4a+5
G4a+6
G4a+7
G4a+8
G4a+9
G4a+10
G4a+11
-1CLK

FIG. 56

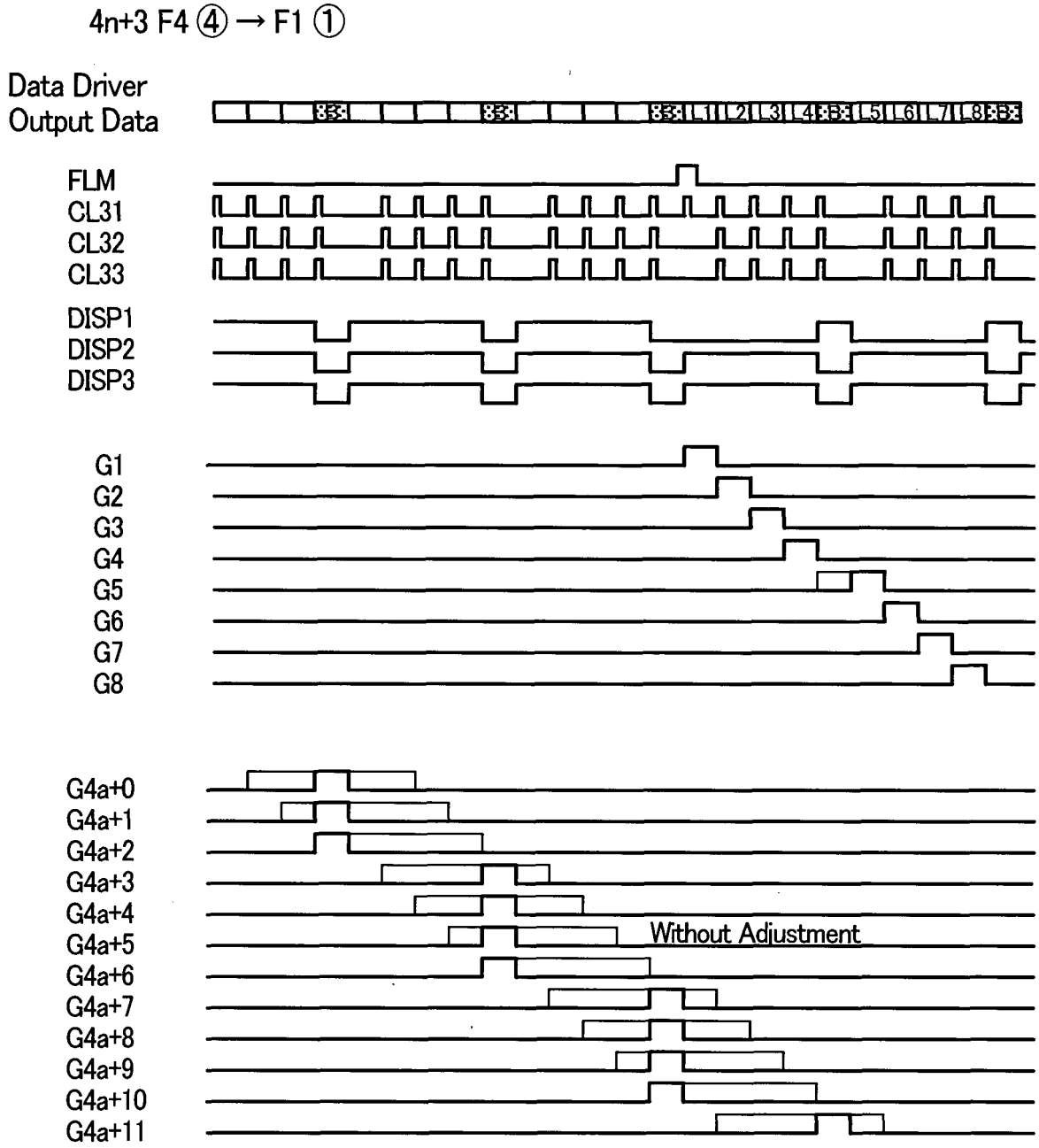

4n+3 F4 ④ → F1 ①
Data Driver Output Data
L1
L2
L3
L4
L5
L6
L7
L8
FLM
CL31
CL32
CL33
DISP1
DISP2
DISP3
G1
G2
G3
G4
G5
G6
G7
G8
G4a+0
G4a+1
G4a+2
G4a+3
G4a+4
G4a+5
G4a+6
G4a+7
G4a+8
G4a+9
G4a+10
G4a+11
Without Adjustment

FIG. 57

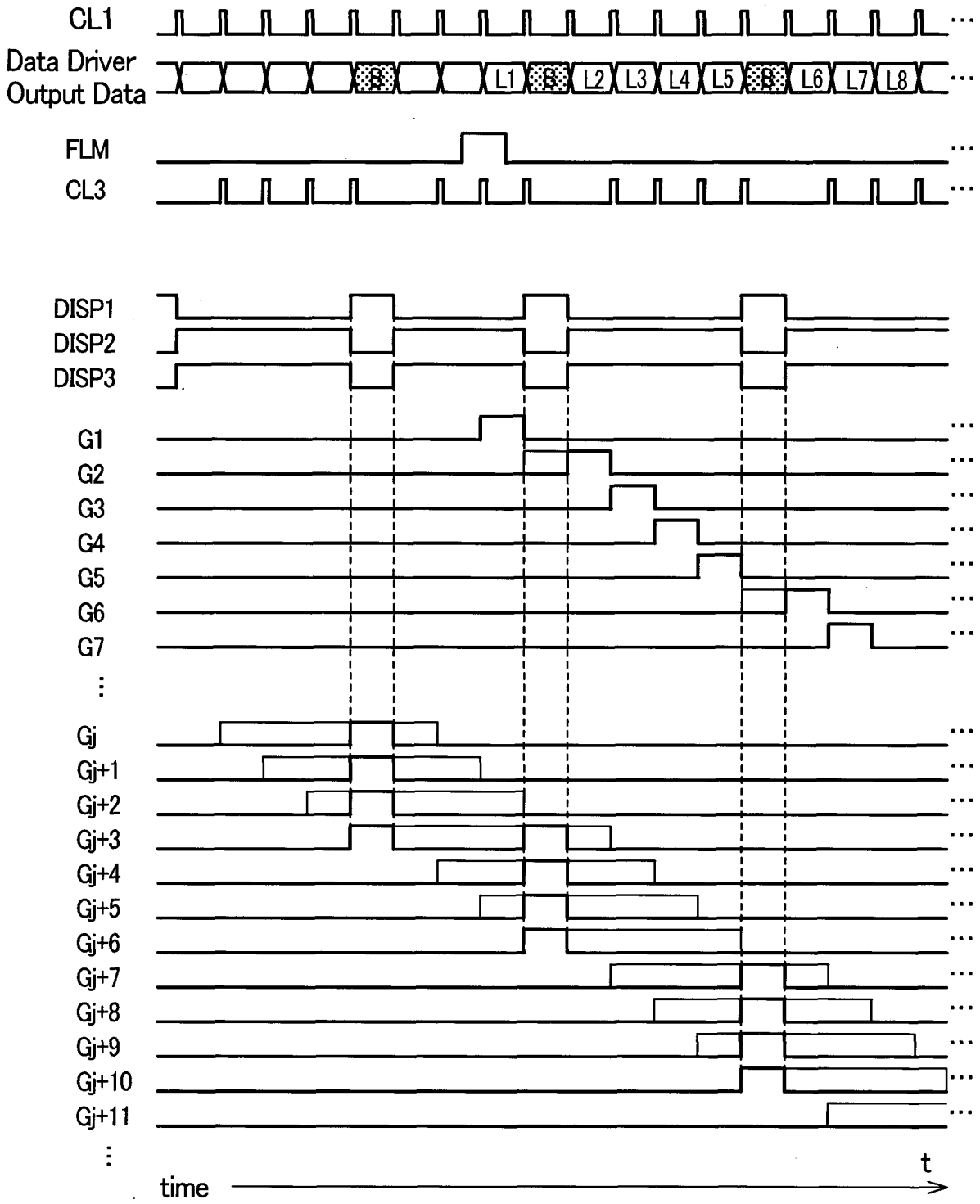
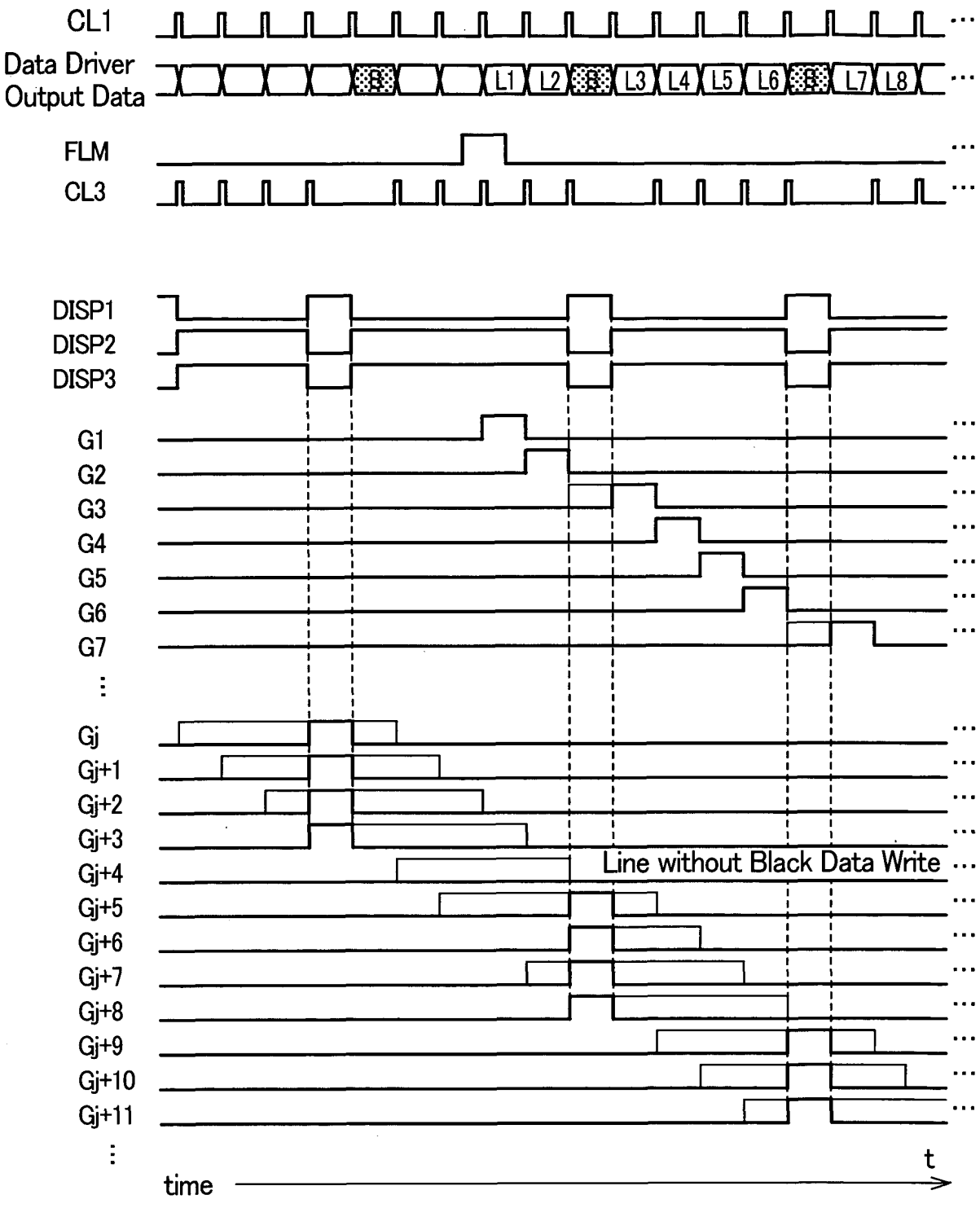

CL1
Data Driver Output Data
FLM
CL3
DISP1
DISP2
DISP3
G1
G2
G3
G4
G5
G6
G7
Gj
Gj+1
Gj+2
Gj+3
Gj+4
Gj+5
Gj+6
Gj+7
Gj+8
Gj+9
Gj+10
Gj+11
L1
L2
L3
L4
L5
L6
L7
L8
time
t

FIG. 58


CL1
Data Driver Output Data
L1
L2
L3
L4
L5
L6
L7
L8
FLM
CL3
DISP1
DISP2
DISP3
G1
G2
G3
G4
G5
G6
G7
Gj
Gj+1
Gj+2
Gj+3
Gj+4
Gj+5
Gj+6
Gj+7
Gj+8
Gj+9
Gj+10
Gj+11
Line without Black Data Write
time
t